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WAVETEK

WAVETEK SAN DIEGO, INC.

9045 Balboa Ave., San Diego, CA 92123

INSTRUCTION MANUAL

MODEL 271
PULSE/FUNCTION
GENERATOR

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SAFETY

This instrument is wired for earth grounding via the facility power wiring. Do not bypass earth grounding with two wire extension cords, plug adapters, etc.

While the very low power of the rf energy generated in this instrument makes it ordinarily nonhazardous, extremely close and prolonged proximity of an eye and an rf output connector could cause injury.

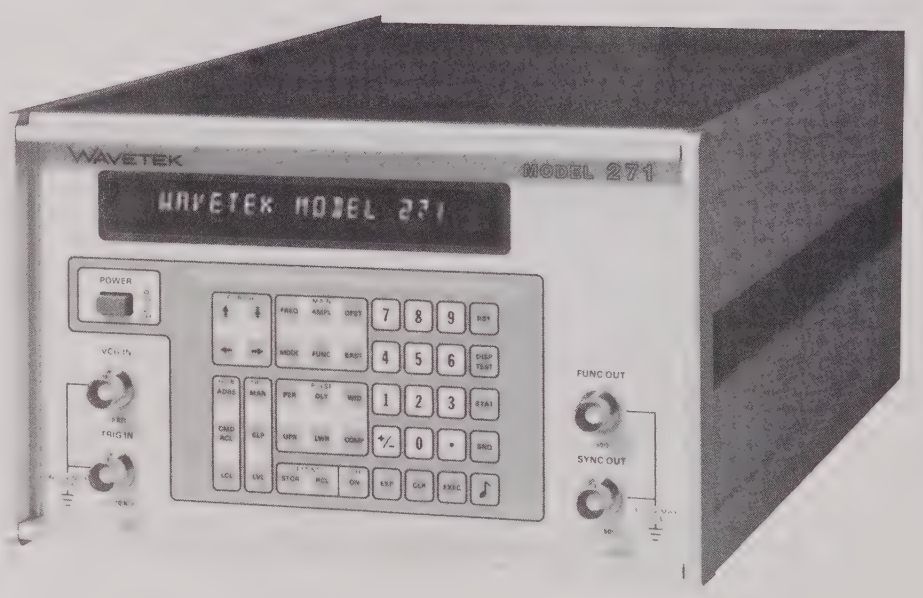
BEFORE PLUGGING IN the instrument, comply with installation instructions.

MAINTENANCE may require power on with the instrument covers removed. This should be done only by qualified personnel aware of the electrical hazards.

The instrument power receptacle is connected to the instrument safety earth terminal with a green/yellow wire. Do not alter this connection. (Reference: ⏚ or ⚠ stamped inside the rear panel near the safety earth terminal.)

WARNING notes call attention to possible injury or death hazards in subsequent operations.

CAUTION notes call attention to possible equipment damage in subsequent operations.



Model 271, Pulse/Function Generator

SECTION 1
GENERAL DESCRIPTION

1.1 MODEL 271

The Wavetek 271 Programmable Pulse/Function Generator produces sine, triangle and square waveforms as well as single or double pulses of programmable delay and width. Any of the waveforms can be generated in the continuous, triggered, gated, or burst modes. External width and dc functions are also provided.

Pulse functions include single (undelayed) pulse, delayed pulse, and double pulse. All pulse waveforms may be complemented.

Data entry is from the front panel or GPIB (IEEE 488-1978). Numeric input is entered in free format: fixed, floating, or exponential notation. Parameters may be entered in any order. Internally, all entries are interactively checked for errors and displayed on the front panel, or they may be accessed through the GPIB.

Output level is specified with 3 digits of resolution from 10 mV to 10 Vp-p into a 50Ω termination and 20 mV to 20 Vp-p into an open circuit. Offset can be programmed to vary the waveform base line up to ± 10V, or in the dc function, to vary the dc output. Output level and offset for all waveforms may also be specified directly in terms of upper and lower peak level.

All inputs and outputs are protected against short circuits and excessive voltages between ± 15V. The function output is further protected against voltage inputs up to 140 Vac or ± 200 Vdc. Activation of the protection circuits will cause a front panel error message and may cause a GPIB service request.

Up to 150 sets of complete front panel settings can be stored in memory. The memory has a non-rechargeable lithium battery back up for a minimum of 6 months (typically 1 to 2 years). A "low battery" warning will be indicated on the display when the battery voltage drops to 80% of its normal voltage.

WARNING

This equipment uses a BR-1/2A, 3V lithium battery, that contains less than 0.3 grams of lithium. To prevent the release of a potentially harmful substance, DO NOT RECHARGE, SHORT CIRCUIT, DISASSEMBLE, OR APPLY HEAT TO THE BATTERY. In addition, observe correct polarity when replacing.

1.2 ACCESSORIES

Rack mounts for a single instrument, rack mounts for two series 270 instruments side-by-side and instrument slides are available accessories. Refer to paragraph 1.3.8 for details.

1.3 SPECIFICATIONS

1.3.1 Main Generator

1.3.1.1 Main Generator Waveforms (Functions)

Programmable sine ∿, triangle ∿, square ⊓, square complement, dc, and external width.

Sine Distortion (THD at Vp-p):
<0.5% 10 mHz to 99.9 kHz.
No harmonics above
– 40 dBc 100 kHz to 999 kHz
– 30 dBc 1 MHz to 12 MHz.

Time Symmetry:
± 1% ± 8 ns.

Square Transition Time:
<15 ns.

Square Overshoot:
<4% at full amplitude.

Triangle Linearity:
99% to 100 kHz.

1.3.1.2 Operational Modes

Continuous:
Output continuous at programmed frequency or period.

Triggered:
Output quiescent until triggered by external signal, internal trigger, GPIB trigger or manual trigger, then generates one cycle at programmed frequency or period.

Gated:
Similar to triggered mode, except that output is continuous for the duration of the gate signal. The last cycle started will be completed.

Burst:
Similar to triggered mode, except that the number of cycles produced is programmable.
Count Range: 1 to 1,048,200.
Burst Rate: 12 MHz maximum.

1.3.1.3 Frequency

Range:
10 mHz to 12 MHz for sine, triangle, square, square complement, >15 MHz for external width.

Resolution:
3 digits.

Accuracy:
± 2%

Repeatability (24 hr):
± 1%

Jitter:
≤0.1% ± 100 ps

Control:
Frequency may be controlled by programmed value, programmed period or external VCG input.

Value:
Frequency value is keyboard or GPIB programmable with automatic range selection.

VCG (Voltage Controlled Generator):
AC or dc input controls frequency. 0.01 to 12V into 10kΩ for up to 1200:1 frequency change in each of 9 frequency ranges (range must be programmed). Slew rate is limited to 1V/μs.

1.3.1.4 Amplitude

Range:
0.01 to 10 Vp-p into 50Ω (0.02 to 20 Vp-p into open circuit) from main output. Absolute peak amplitude plus offset may not exceed 5V into 50Ω (10V into open circuit). Amplitude and offset may also be specified directly in terms of upper and lower peak waveform level.

Resolution:
3 digits or 10 mV when absolute peak amplitude plus offset >0.5V; 3 digits or 1 mV when absolute peak amplitude plus offset ≤0.5V.

Accuracy:
± 2% of programmed value and:
± 5 mV for 0.1 to 1V (peak amplitude + offset <0.5V),
± 20 mV for 1.01 to 10V,
± 50 mV for all other.

Repeatability (24 hr):
± 1% ± 10 mV.

Flatness (at 5 Vp-p):
0.1 dB to 100 kHz, 1.5 dB to 12 MHz.

Control:
Vp-p and offset, or upper and lower peak voltage.

1.3.1.5 Offset

Range:
DC or offset programmable from − 5V to + 5V into 50Ω (− 10V to + 10V into open circuit). Absolute peak amplitude plus offset may not exceed 5V into 50Ω (10V into open circuit). Amplitude and offset may also be specified directly in terms of upper and lower peak waveform level.

Resolution:
3 digits or 10 mV when absolute peak amplitude plus offset >0.5V, 3 digits or 1 mV when absolute peak amplitude plus offset ≤0.5V.

Accuracy:
± 40 mV in dc function.

Repeatability (24 hr):
± 20 mV.

1.3.2 Pulse Generator

1.3.2.1 Pulse Functions

(All pulse functions are available in the continuous, triggered, gated and burst modes.)

Single Pulse:
Single undelayed pulse of programmable width.

Delayed Pulse:
Single pulse of programmable width and delay. Programmed delay is with respect to SYNC OUT signal.

Double Pulse:
Double pulse of programmed width, with programmable delay between pulses.

1.3.2.2 Pulse Complement

All pulse functions are available in either normal (uninverted) or complement (inverted) phase.

1.3.2.3 Pulse Period

Range:
83.3 ns to 100 seconds. Pulse period may also be programmed in terms of frequency.

Accuracy and Repeatability:
Same as main generator frequency.

1.3.2.4 Pulse Delay and Width:

Delay Range
80 ns to 100 ms. Measured from 1.25V point of leading edge of SYNC OUT signal (into 50Ω load) to leading corner of main output pulse. (In double pulse, to second pulse of pulse pair.)

Width Range:
40 ns to 100 ms. Measured from 50% of leading edge to 50% of trailing edge.

Delay Duty Cycle:
Delay may not be greater than 50% of period when delay is programmed to be less than 500 ns. For a programmed delay of 500 ns or greater, the maximum allowable delay is 80% of period.

Width Duty Cycle:
Width may not be greater than 50% of period when width is programmed to be less than 500 ns. For a programmed width of 500 ns or greater, the maximum allowable width is 80% of period.

Delay and Width Resolution:
3 digits.

Delay and Width Accuracy:
±3% of programmed value ±10 ns.

Delay and Width Repeatability (24 hr):
±1% ±3 ns.

1.3.3 Outputs

Function Output:
Source of primary and pulse waveforms.

Program control provides:

Output on, 50Ω source impedance;
Output off, high Z (>500kΩ);
Output off, low Z (terminated in approximately 50Ω).

Protection: Output protected to 140 Vac or 200 Vdc without internal damage.

Sync Output:
TTL level sync signal at programmed frequency.

Level:

≤0.4V to ≥2.4V into 50Ω,
≤0.8V to ≥4.8V into open circuit.

Source Impedance: 50Ω.

Timing: Concurrent with function output for square and pulse functions; lags sine and triangle waveforms by 90°.

Over/Undershoot: <10% into 50Ω.

Protection: Output protected from short circuit to any voltage between ±15 Vdc.

1.3.4 Inputs

External Trigger:
Trigger of input circuit is programmable for a + or − signal slope and required threshold level.

Level: −10 to +10V.

Resolution: 20 mV.

Accuracy: ±500 mV.

Input Impedance: 10 kΩ.

Maximum Trigger Rate: 12 MHz (15 MHz for External Width function).

Minimum Trigger Width: 20 ns.

Minimum Amplitude: 500 mVp-p to 1 MHz, 1 Vp-p to 15 MHz.

Protection: Input protected to ±50V.

VCG in:
Voltage control of generator frequency. See Frequency.

Range: 0.01 to 12V.
Impedance: 10kΩ.
Protection: Input protected to ±50V.

1.3.5 GPIB Programming

IEEE 488-1978 compatible. Nonisolated. Double buffered.

Address:
0-30, keyboard or internal switch selectable. Internal switch can lock out keyboard selection. Power-up address is internal setting.

Subsets:
SH1, AH1, T6, TE0, L4, SR1, RL1, PP0, DC1, C0, E2.

Interface Timing:

Frequency	11 ms
Amplitude	14 ms
Offset	14 ms
Mode	4 ms
Function	5 ms
Execute	8 ms
Other	4 ms

1.3.6 General

Stored Settings:
Non-volatile memory for 150 stored settings.

Environmental:

Temperature Range: 25°C ±10°C for specified operation; operates 0°C to 50°C; −50°C to +75°C for storage.

Altitude: Sea level to 10,000 ft for operation. Sea level to 40,000 ft for storage.

Relative Humidity: 95% at 20°C at sea level (non-condensing).

Warm-up Time:
20 minutes for specified operation.

Dimensions:
21.7 cm (8.54 in) wide (half-rack); 13.3 cm (5.25 in) high; 39.4 cm (15.5 in) deep.

Weight:
5.9 kg (13 lb) net, 7.2 kg (16 lb) shipping.

Power:
90 to 105, 108 to 126, 198 to 231, or 216 to 252 volts rms; 48 to 66 Hz, 1 phase; <40 watts.

1.3.7 Options

002: Rear Panel Connectors
Front panel BNC connectors relocated to rear panel.

1.3.8 Accessories

Style 12: Single Rack Adapter Kit
Allows right or left mounting in a standard 19 inch rack. 5¼ inches high.

Style 13: Dual Rack Adapter Kit
Allows any 270 series instrument to be mounted side-by-side in a standard 19 inch rack. 5¼ inches high.

Rack Slides

SECTION 2
INSTALLATION & INTERFACE

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

The generator can be used as a bench instrument or rack mounted. The 271 can be converted to rack mounts in the field by using the following kits.

Rack Mount Kit	Part Number	Reference Drawing
Single Instrument (left and right mounting)	1101-00-1043	0102-00-1043
Dual Instruments	1101-00-1041	0102-00-1041
Rack Slides	1101-00-1042	0102-00-1042

NOTE

The rack slides can only be used with dual rack mounted instruments.

Whether used on a bench or in a rack, ensure that there is no impedance to air flow at any surface of the instrument. Before rack mounting, it may be desirable to perform the initial checkout (paragraph 2.2.5) to verify operation of all functions.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 120 Vac line supply and with a ½ amp fuse.

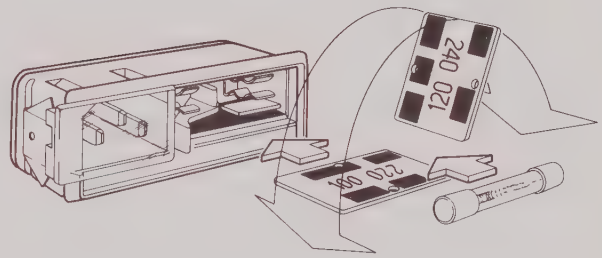


Figure 2-1. Voltage Selector and Fuse

Conversion to other input voltages requires a change in rear panel fuse holder voltage card position and fuse (figure 2-1) according to the following procedure.

1. Disconnect the power cord at the instrument, open fuse holder cover door and rotate fuse-pull to left to remove the fuse.
2. Remove the small printed circuit board and select operating voltage by orienting the printed circuit board to position the desired voltage to the top left side. Push the board firmly into its module slot.

Card Position	Input Vac	Fuse
100	90 to 105	½ amp
120	108 to 126	½ amp
220	198 to 231	¼ amp
240	216 to 252	¼ amp

3. Rotate the fuse-pull back into the normal position and insert the correct fuse into the fuse holder. Close the cover door.
4. Connect the ac line cord to the mating connector at the rear of the unit and the power source.

3. Rotate the fuse-pull back into the normal position and insert the correct fuse into the fuse holder. Close the cover door.

4. Connect the ac line cord to the mating connector at the rear of the unit and the power source.

2.2.2 Signal Connections

NOTE

Use RG58U 50Ω or equivalent 50Ω coaxial cables equipped with BNC connectors to distribute signals.

Instrument BNC connectors are:

TRIG IN. Acceptable trigger characteristics of level and slope are programmable; 10 kΩ impedance.

SYNC OUT. TTL level square wave; 50Ω impedance

FUNC OUT. Up to 10 Vp-p into 50Ω impedance; up to 20 Vp-p into >50 kΩ impedance.

VCG IN. 0.01 to 12V; 10 kΩ impedance.

Signal ground may be floated up to ±42 volts with respect to chassis ground. Be aware that all signal grounds are common; thus, if one signal ground requires floating, all grounds must be floated together.

2.2.3 GPIB Connections

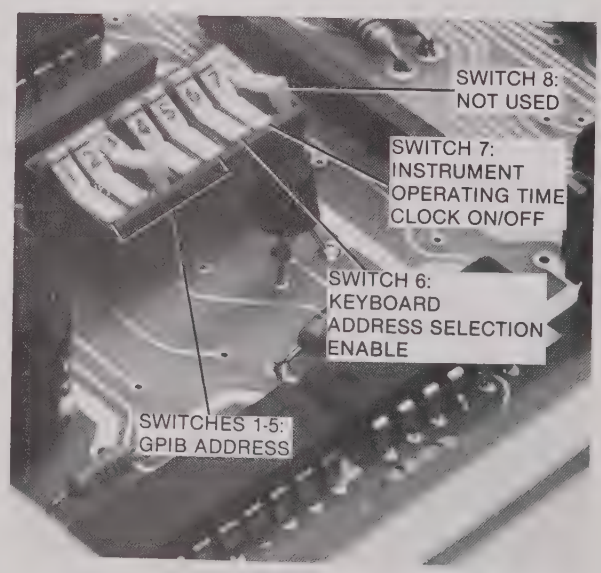
The GPIB I/O rear panel pin connections and signal names are given in table 2-1. The panel connector is an Amphenol 57-10240 or equivalent and connects to a GPIB bus cable connector (available from Wavetek in 1 and 2 meter lengths).

2.2.4 GPIB Address

For instruments on the General Purpose Interface Bus (GPIB), ensure that the instrument GPIB address is correct. The GPIB address can be changed by the internal switch (for access, remove the bottom cover, see figure 2-2) or the front panel GPIB ADRS key (e.g., ADRS 4 EXEC). The switch sections are labeled from 1 through 5 and their OFF position noted (OFF = Binary "0" in table 2-2). To verify the address, press ADR on the front panel. The device number (decimal) will be displayed. Upon power-up, the address is always that of the internal switch.

Table 2-1. GPIB Data In/Out

Pin	Signal	
1	DIO1	True When Low
2	DIO2	
3	DIO3	
4	DIO4	
5	EOI	
6	DAV	
7	NRFD	True When High
8	NDAC	
9	IFC	True When Low
10	SRQ	
11	ATN	
12	Chassis Ground (⏚)	
13	DIO5	True When Low
14	DIO6	
15	DIO7	
16	DIO8	
17	REN	
18		Signal Ground (⏚)
19		
20		
21		
22		
23		
24		



NOTE: GPIB ADDRESS SELECTED IS DECIMAL 4: SWITCH 1 OFF, 2 OFF, 3 ON, 4 OFF, 5 OFF. (TABLE 2-2: 00100)

Figure 2-2. GPIB Address Selector Switch

Table 2-2. GPIB Address Codes

	ASCII		Switch Position	Hexa-decimal	
Device	**Listen**	**Talk**	**1 2 3 4 5**	**Listen**	**Talk**
0	(space)	@	0 0 0 0 0	20	40
1	!	A	1 0 0 0 0	21	41
2	"	B	0 1 0 0 0	22	42
3	#	C	1 1 0 0 0	23	43
4	$	D	0 0 1 0 0	24	44
5	%	E	1 0 1 0 0	25	45
6	&	F	0 1 1 0 0	26	46
7	'	G	1 1 0 0 0	27	47
8	(	H	0 0 0 1 0	28	48
9	)	I	1 0 0 1 0	29	49
10	*	J	0 1 0 1 0	2A	4A
11	+	K	1 1 0 1 0	2B	4B
12	,	L	0 0 1 1 0	2C	4C
13	—	M	1 0 1 1 0	2D	4D
14	•	N	0 1 1 1 0	2E	4E
15	/	O	1 1 1 1 0	2F	4F
16	0	P	0 0 0 0 1	30	50
17	1	Q	1 0 0 0 1	31	51
18	2	R	0 1 0 0 1	32	52
19	3	S	1 1 0 0 1	33	53
20	4	T	0 0 1 0 1	34	54
21	5	U	1 0 1 0 1	35	55
22	6	V	0 1 1 0 1	36	56
23	7	W	1 1 1 0 1	37	57
24	8	X	0 0 0 1 1	38	58
25	9	Y	1 0 0 1 1	39	59
26	:	Z	0 1 0 1 1	3A	5A
27	;	[	1 1 0 1 1	3B	5B
28	<	\	0 0 1 1 1	3C	5C
29	=	]	1 0 1 1 1	3D	5D
30	>	^	0 1 1 1 1	3E	5E

NOTE

Address 31 is not allowed.

2.2.5 Initial Checkout and Operation Verification

Make the equipment setup as shown in figure 2-3 and perform the steps in table 2-3 to verify Model 271 operation. If further explanations are required, refer to figure 3-1 and table 3-1.

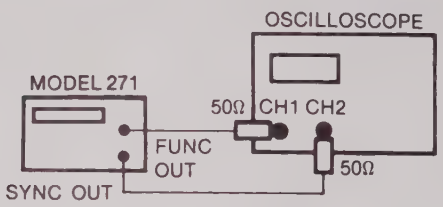


Figure 2-3. Setup

Table 2-3. Initial Checkout

Step	Test	Tester & Setup	Program	Desired Results
1	Wake-up State	Connect Model 271 and oscilloscope as shown in figure 2-3. Scope setting: CH1 2 V/div, CH2 2V/div; horizontal 0.2 ms/div; trigger on CH2.	Power: ON	Display: All segments, decimal points and commas light up for 1 second, then WAVETEK MODEL 271.
2	Wake-up Status		Press STAT key	Display (changes automatically): FREQ 1 KHz AMPLITUDE 5V OFFSET 0V MODE CONTINUOUS (0) FUNC SINE (0) BURST COUNT 2 PERIOD 1 mS DELAY 120 nS WIDTH 40 nS UPPER LEVEL 2.5V LOWER LEVEL −2.5V PULSE NORMAL (0) OUTPUT OFF (0) TRIG SLOPE POS (0) TRIG LEVEL 1.5V
3	Status Search		STAT	Status display sequence stops.
4			↑	Status progresses forward.
5			↓	Status progresses backward.
6			STAT	Status display automatic sequence continues.
7	Display Test		DISP TEST	All segments, decimal points and commas light up. Back to last display when released.
8			Press FREQ key a few times	Beeper sounds every time key is pressed.
9			Press ↶, then FREQ key a few times	Beeper is silent.

Table 2-3. Initial Checkout (Continued)

Step	Test	Tester & Setup	Program	Desired Results
10		Connect Model 271 and oscilloscope as shown in figure 2-3. Scope setting: CH1 2 V/div, CH2 2V/div; horizontal 0.2 ms/div; trigger on CH2.	↙	Beeper enabled.
11	Command Recall		Press each of the 6 keys in the MAIN generator section 4 times then CMD RCL.	Strings of characters shown on display. Characters are the ones shown on lower left of each key.
12			Press → then ←	Moves characters right then left 4 at a time.
13	GPIB Address And Status		ADRS 1 EXEC then 30 EXEC	Display: GPIB ADRS 1 then GPIB ADRS 30
14	Quality Assurance Procedure		Press: RCL 2000 EXEC	Display: (0) BEGIN QA PROC Scope: CH1, 5 Vp-p 1 kHz sine wave. CH 2, 2.5 Vp-p 1 kHz square wave
15	Frequency: Exercises Each Frequency Bit and the Sine Wave Function		Press: CURSOR ↑ once.	Display: (1) FREQUENCY. Scope: CH1, 5 Vp-p sine wave continuously sweeping from 1 kHz to 10 kHz. CH2, 2.5 Vp-p square wave synchronous with CH1.
16	Amplitude: Exercises Each Amplitude Bit and the Triangle Wave Function.		Press: CURSOR ↑ once.	Display: (2) AMPLITUDE Scope: CH1 1 kHz triangle wave, amplitude continuously increases from 1V to 10 Vp-p. CH2, 2.5 Vp-p square wave synchronous with CH1.
17	Offset: Exercises DC Offset Bit and Offset Bit and Square Function.		Press: CURSOR ↑ once.	Display: (3) OFFSET Scope: CH1 1 Vp-p square wave. DC offset continuously increases from −4V to +4V. CH2, 2.5 Vp-p square wave synchronous with CH1.
18	Delay Circuit		Press CURSOR ↑ once.	Display: (4) DELAY Scope: CH1 5 Vp-p 100 μs pulse, delay continuously increasing from 120 μs to 780 μs. CH2 2.5 Vp-p 1 kHz square wave.
19	Width Circuit		Press: CURSOR ↑ once.	Display: (5) WIDTH Scope: CH1 5 Vp-p pulse, width continuously increasing from 140 μs to 780 μs. CH 2 2.5 Vp-p 1 kHz square wave.
20	Trigger Circuit	Trigger Scope on CH1.	Press: CURSOR ↑ once.	Display: (6) TRIGGER Scope: CH1, 5 Vp-p 1 ms pulse. CH2 2.5 Vp-p 100 μs pulse, delayed 50 μs relative to positive edge CH1.

Table 2-3. Initial Checkout (Continued)

Step	Test	Tester & Setup	Program	Desired Results
21	Gate Circuit	Trigger Scope on CH1.	Press CURSOR ↑ once.	Display: (7) GATE Scope CH1 5V p-p 1 ms pulse. CH2 2.5 Vp-p Pulse burst: six 100 μs pulses.
22	Burst Circuit		Press: CURSOR ↑ once.	Display: (8) BURST Scope: CH1 5 Vp-p pulse with pulse width continuously varying between 1.6 and 0.2 ms. CH2 2.5 Vp-p 100μs pulse continuously varying in number between 9 and 2.
23			Press: CURSOR ↑ once.	Display: (9) END QA PROC.

SECTION 3
OPERATION

3.1 INTRODUCTION TO OPERATION

The Wavetek 271 may be operated either locally, from the front panel keyboard, or remotely, via the GPIB (General Purpose Interface Bus). This manual presents local operation first, then additional information required for remote operation. Users who plan to control the instrument remotely should read *both* sections.

3.2 FRONT PANEL CONTROLS AND CONNECTORS

The front panel contains the power switch, keyboard, display and (unless option 002, rear panel connectors, has been specified) the BNC signal connection jacks. Figure 3-1 shows the location of all front panel controls and connectors. Table 3-1, which is keyed to the numeric identifiers in Figure 3-1, briefly lists the purpose of each control or connector for quick reference. Further information on the controls is contained in section 3.4, LOCAL OPERATION.

3.3 POWER-UP

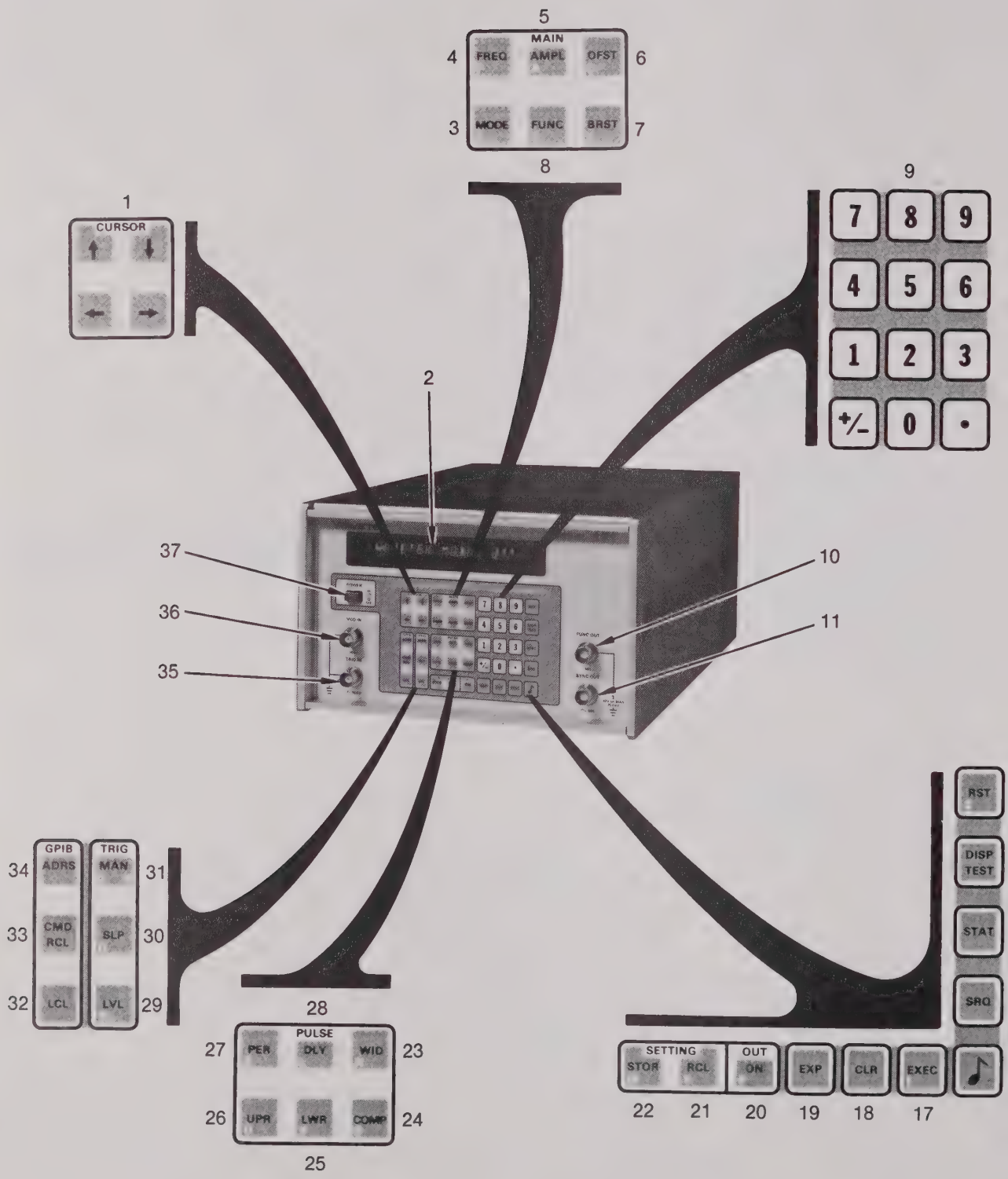
When ac power is applied to the instrument, the microprocessor performs internal checks and initializes the internal circuitry. During the first second, the microprocessor performs a display test by lighting all display segments and punctuation marks. When the initialization is complete,

is displayed. During power-up, all parameters are set to default values.

Table 3-1. Controls and Connectors

Key Ref No.	Control or Connector	Description
1	CURSOR	← and → position the cursor to any numerical digit (indicated by the flashing digit on the display). ↑ and ↓ increment or decrement codes, storage addresses or the flashing digit (features carry action) of a parameter value. ← and → are also used to move a displayed program string (CMD RCL) to the left or right in increments of 4 characters. Because ↑ and ↓ employ an automatic execute, the instrument output is instantly changed with cursor action.
2	DISPLAY	Twenty character readout (both manually and remotely accessible). Advises operator of parameters and values, errors, warnings and GPIB activity. Also displays programming strings.
3	MODE (B)	Displays main generator modes and enables change. There are four basic modes.

MODE	CODE
Continuous	0
Triggered	1
Gated	2
Burst	3



NOTE: Features are keyed to Table 3-1

Figure 3-1. Controls and Connectors

Table 3-1. Controls and Connectors (Continued)

Key Ref No.	Control or Connector	Description
4	FREQ (F)	Displays generator frequency and enables change. Generator frequency is 10 mHz to 12 MHz with 3 digit resolution.
5	AMPL (A)	Displays output amplitude programming and enables change. Amplitude maximum is 10.00 Vp-p into 50Ω. Open-circuit amplitude will be approximately twice as high.
6	OFST (D)	Displays dc offset programming and enables change. DC offset used with amplitude adjusts the output waveform offset bias. Maximum offset is ± 5V into 50Ω.
7	BRST (R)	Displays burst count and enables change. Burst count can be from 1 to 1,048,200. This is the number of waveform cycles in the burst each time it is triggered.
8	FUNC (C)	Displays function (waveform) programming and enables change. Function may be one of nine output waveforms.

FUNCTION	CODE
Sine	0
Triangle	1
Square	2
Square Complement	3
DC	4
External Width	5
Single Pulse	6
Delayed Pulse	7
Double Pulse	8

9	NUMERICAL KEYBOARD	Used with other keys to enter data or retrieve information. Free format data entry allows fixed point, floating point and scientific (exponential) notation. Microprocessor will round off as required.
10	FUNC OUT	The main output of selected waveforms. Function output is off at power-up and reset. Output control key 20 sets FUNC OUT on or off with 50Ω impedance.
11	SYNC OUT	The sync signal has the same frequency as FUNC out signal and is 0V to >2.4V (TTL level) into a 50Ω load (>4.8V open circuit).
12	RST (Z)	Returns the instrument waveform parameters to their power-on condition. Stored settings are not affected.
13	DISP TEST	Lights all 20 sets of character segments.

Table 3-1. Controls and Connectors (Continued)

Key Ref No.	Control or Connector	Description
14	STAT	Gives the current waveform generator status by displaying each parameter and value momentarily. Pressing the key a second time holds the display.
15	SRQ	To use the SRQ key, the instrument must be in the local mode and the SRQ mode bit 128 must have previously been selected by remotely programming an SRQ mode of XQ128 or higher (XQ255 maximum). Under these conditions pressing the SRQ key asserts the SRQ line of the GPIB.
16	♪	Turns audible tone on or off. If there is no tone when key is pressed, pressing ♪ restores the tone.
17	EXEC (I)	Causes all the entered instructions to be error checked and transferred to waveform circuits. No parameter entries will change the output until execute (EXEC key, CURSOR ↑, CURSOR ↓, GPIB I, GPIB GET, GPIB Z or RESET) is received. This permits a complete test setup to occur at one time with no in-between parameter change aberrations.
18	CLR	Corrects front panel and scratch-pad numerical entries. (An asterisk on the display indicates that the value displayed has not been executed and resides in scratch-pad memory only.)
19	EXP (E)	Designates the next numerical and +/− entries pertaining to the power of the X10 multiplier.
20	OUT ON (P)	Displays output and load status and enables change. Output status programming codes are:

OUTPUT	CODE
Output Off (0) (>100kΩ)	0
Output On (1) (50Ω)	1
Output Off, Lo Z (2) (≅50Ω)	2

21	RCL (Y)	Displays the status of setting recall (none recalled, recall setting No. _____, or No. _____ last recalled) and enables the change of address of settings to be recalled. Stored settings can be recalled to scratch-pad memory only and do not affect the instrument output operation if recall is alpha terminated but not executed. Recall settings and selections are:

SETTINGS	RCL
Recall last power off condition	0
Recall user-stored settings	1-150
Internal calibration procedure	1000-1039
Internal QA test/demo procedure	2000-2009

Table 3-1. Controls and Connectors (Continued)

Key Ref No.	Control or Connector	Description
22	STOR (M)	Displays address of last storage location used and enables storage location address change. The settings stored are those currently in scratch-pad memory; the instrument output operation is not disturbed by storage action. Entry of a negative address erases the stored settings at that address from memory. There are 150 non-volatile stored settings.
23	WID (N)	Displays selected pulse width and enables change. Pulse width is programmable from 40 ns to 100 ms.
24	COMP (0)	Selects normal or inverted pulse output

PULSE PHASE	CODE
Normal	0
Inverted	1

Key Ref No.	Control or Connector	Description
25	LWR (V)	Displays programmed value of negative peak of FUNC OUT waveform for all waveform functions except DC (4) and enables entry of new value. Lower level must be programmed to be less than upper level.
26	UPR (U)	Displays programmed value of positive peak of FUNC OUT waveform for all waveform functions except DC (4) and enables entry of new value. Upper level must be programmed to be greater than lower level.
27	PER (S)	Displays pulse period (repetition time) and enables change. Programmable period range is 100 seconds to 83.3 ns.
28	DLY (L)	Displays selected pulse delay (with respect to SYNC OUT signal) and enables entry of new value. Delay range is 80 ns to 100 ms. This parameter is applicable only to the delayed pulse (7) function and the second pulse of the double pulse (8) function. It is not applicable to the undelayed single pulse (6) function.
29	LVL (XL)	Displays programmed trigger level and enables change. Trigger level is the voltage at which the trigger circuit is sensitive to the TRIG IN BNC input signals. Trigger level may be set in the ±10 Vdc range with 20 mV resolution.
30	SLP (Q)	Displays select slope and enables change. Selects generator triggering on the rising or falling edge of the TRIG IN BNC signal.

TRIGGER	CODE
Positive slope	0
Negative slope	1

Table 3-1. Controls and Connectors (Continued)

Key Ref No.	Control or Connector	Description
31	MAN TRIG (J) (H)	Triggers or gates the instrument if triggered, gated or burst mode has been selected. The two ASCII codes (J and H) are for gating; J gates on and H gates off.
32	LCL	Takes the instrument out of remote control (without affecting the rest of the bus) and places it under front panel control. This key can be locked out from the GPIB controller with the LLO (local lockout) command if so desired.
33	CMD RCL	Displays the last 40 parameters, values and actions (all in ASCII code) sent to the instrument from the keyboard and the GPIB. The display shows only 20 characters at a time, and the CURSOR ← and → must be used to see the entire 40 character string.
34	(GPIB) ADRS	Displays the GPIB decimal address and enables change, with the following exception: The GPIB address cannot be changed by front panel control if the internal disable switch has been set.
35	TRIG IN	Connector for external trigger signal. A sufficient external signal level transition triggers or gates the generator when generator mode requires a trigger or gate signal. The required level is determined by key 29 and the required transition by key 30.
36	VCG IN	The VCG input accepts ac or dc voltages used to externally control the frequency of the generator. A positive voltage applied to the VCG IN connector will increase the generator frequency; a negative voltage will decrease the frequency. 0.01V to 12V gives approximately 1200:1 frequency change. Input impedance is 10 kΩ.
37	POWER ON/OFF	Turns generator on or off.

3.4 LOCAL OPERATION

Local operation is accomplished from the front panel keyboard. The front panel keys fall into three general categories:

1. Action keys, which cause an immediate action when pressed.
2. Parameter keys, which display the current value of a parameter (such as frequency), but do not cause any action until a new value is entered.
3. Numeric keys, which are used for entry of numeric data. These keys are [0] through [9], [+/-], [•] and [EXP].

Many of the keys are labelled with an alphabetic character in addition to the name of the key function. These alphabetic characters are for reference in remotely controlling the instrument, and for reading back previous commands from the display with the [CMD RCL] key. (The [EXP] key is associated with the ASCII character "E", but this letter is not marked on the key.) Appendix B, Programming Command Summary, lists the ASCII character associated with each key, and also lists ASCII commands for which there is no equivalent keyboard key. Remote operation will be covered in section 3.5 of the manual.

3.4.1 Action Keys

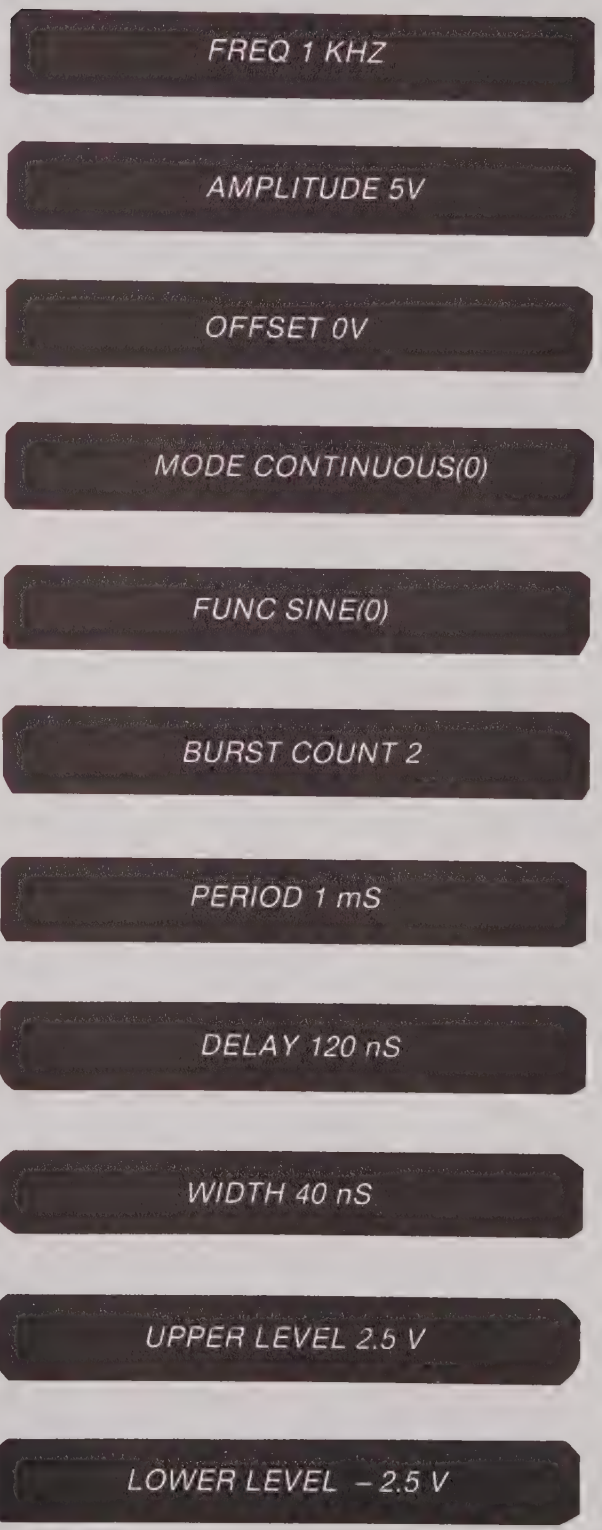
The keys that cause an immediate action when pressed and do not require entry of a numerical parameter value are the CURSOR keys, RESET, DISPLAY TEST, STATUS, SRQ, Tone, EXECUTE, CLEAR, LOCAL and COMMAND RECALL.

3.4.1.1 Tone Key

An audible tone indicates that a key is pressed. Pressing [♪] will inhibit or enable the key tone. If there is no tone when keys are pressed, pressing [♪] restores the tone.

3.4.1.2 Status Key

Pressing [STAT] (the status key) will cause the display to sequentially indicate the current instrument parameters. At power on or reset, the following parameters will be displayed:



By pressing [STAT], the display will stop on the existing readout, and the status display may be incremented forward or backwards with the [↑] or [↓] CURSOR keys. Holding down the [↑] or [↓] key will cause the display to continuously increment or decrement.

NOTE: the [STAT] key displays only the actual operating parameters of the instrument, not parameters that may be temporarily stored in scratch-pad memory and not yet executed.

3.4.1.3 Cursor Keys

The cursor keys [↑], [↓], [←] and [→] are used to modify a parameter value and cause immediate execution of the new value. The [↑] and [↓] keys are used to increment or decrement a parameter value. Holding the key down continuously causes the value to continuously increment or decrement.

The [←] and [→] keys are used to select which digit of a multiple digit parameter will be incremented or decremented. The selected digit will flash alternately bright and dim on the display. Some parameters, such as [8RST R], can only be incremented or decremented in steps of 1, and the [←] and [→] keys will have no effect when this parameter is selected. Also, these keys will have no effect on a parameter that contains single-digit values, such as mode or function.

3.4.1.4 Reset Key

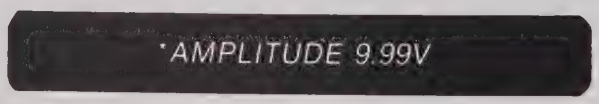
The [RST Z] (Reset) key returns the instrument waveform parameters to their power-on default values. This key does not affect stored settings, or COMMAND RECALL memory.

3.4.1.5 Execute Key

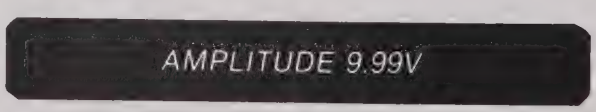
The [EXEC I] (Execute) key transfers all data from the scratch-pad memory to the waveform circuit memory. (A leading asterisk (*) on the display indicates that the parameter value has not been executed.)

Example: Press [AMPL A] [9] [•] [9] [9]. A dash at the end of the string of characters means that the string of characters has not been terminated (nor executed). The display will show

Press [AMPL A] again. The display will be



Press [EXEC I]. The display will change to



3.4.1.6 Clear Entry Key

The [CLR] (Clear) key erases a parameter value which has been entered but not executed. The [CLR] key removes the numeric digits entered after the last parameter key. (Clearable entries are always prefixed

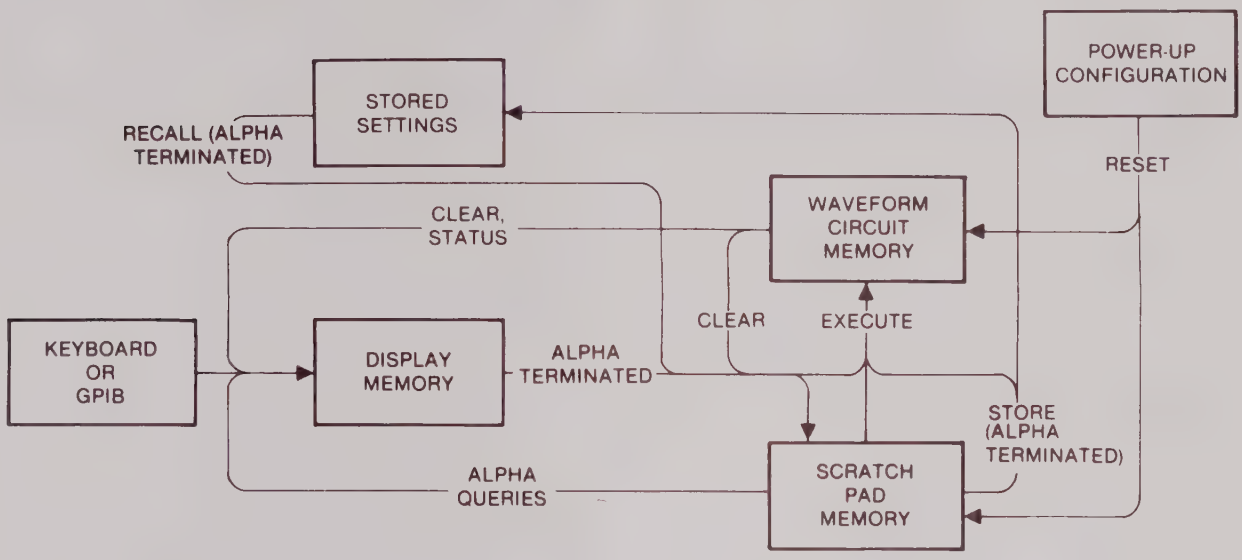


Figure 3-2. Memory Structure

by an asterisk or suffixed by a dash.) The display reverts to that caused by the previous accepted value of the parameter being programmed.

3.4.1.7 Local Key

The [LCL] (Local) key removes the instrument from the bus command and places it under front panel control. This key can be locked out from the GPIB controller with the LLO command if so desired.

3.4.1.8 SRQ Key

The [SRQ] key asserts the SRQ line of the GPIB if the key has been enabled by the GPIB controller. Further information will be found in the REMOTE OPERATION section of the manual (section 3.5).

3.4.1.9 Command Recall Key

Pressing the [CMD RCL] (Command Recall) key displays the last 20 commands from the keyboard or GPIB in the form of ASCII characters. Keyboard commands not associated with an ASCII character (such as the cursor keys) are not shown. The display shows *all* commands associated with an ASCII character, even if the command is erroneous or has been superseded by a later command.

Example: Press [MODE B] [0] [FUNC C] [1] [AMPL A] [2] [OFST D] [3] [FREQ F] [1] [0] [0] [EXEC I].

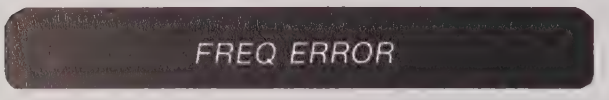
Press [FUNC C] [0] [FREQ F] [1] [EXP] [3] [EXEC I].

Press [CMD RCL]. The display will show:

```
B0C1A2D3F100IC0F1E3I
```

The letters B, C, A, D, F, E and I are the ASCII codes for mode, function, amplitude, offset, frequency, exponent, and execute respectively. Note that the display contains two commands for function and frequency, but that only the last command for each parameter is the actual instrument setting. The ASCII codes for most parameters are shown on the keys. The exception in the above example is exponent.

Now press [FREQ F] [1] [EXP] [9] [EXEC I]. The display will indicate



Press [CMD RCL]. The last 5 characters on the display will be "F1E9I", even though the frequency command was outside the frequency range of the instrument.

Using the cursor [←] and [→] key shifts the display 4 characters to the left or right to allow the eventual display of up to 40 characters.

NOTE

If the [CMD RCL] key is pressed immediately after turning on the instrument, the display will be blank because no characters have been programmed.

3.4.1.10 Display Test Key

The [DISP TEST] key turns on all segments (including punctuation marks) of the front panel display. It has no effect on the instrument output.

3.4.2 Parameter Keys

The parameter keys allow display of a current parameter value, modification of the current value with the cursor keys, or entry of a new value using the numeric keys. The parameter keys are functionally grouped as controls for main waveform, trigger, stored settings, output, GPIB and pulse.

3.4.2.1 Main Waveform Controls

The MAIN block of controls contains the parameter keys for frequency, amplitude, offset, mode, function and burst count.

3.4.2.1.1 Frequency Key

The [FREQ F] key selects waveform frequency in cycles per second. (This parameter may also be entered as a function of time by the [PER S] key instead of the [FREQ F] key.)

3.4.2.1.2 Amplitude Key

The [AMPL A] key selects output waveform amplitude in volts peak-to-peak into a 50Ω load. The waveform will be symmetrical about the selected offset voltage. Amplitude range (with no offset) is 10 mV to 10V peak-to-peak into a 50Ω load. Open-circuit amplitude will be approximately twice as high. (This parameter may also be entered by specifying the upper and lower peak levels directly with the [UPR U] and [LWR V] keys instead of the [AMPL A] and [OFST D] keys.)

3.4.2.1.3 Offset Key

The [OFST D] key selects output waveform offset in volts. Offset is the voltage (into a 50Ω load) midway between the waveform amplitude peaks. (Offset voltage into a high-impedance load is approximately twice as high.) For example, to obtain a square wave having voltage levels of 0V and + 5V, program an amplitude voltage of 5V and an offset voltage of 2.5V. To avoid output clipping, offset voltage plus peak amplitude (p-p amplitude/2) must not exceed 5V. To avoid loss of amplitude resolution, amplitudes less than 100 mV require an offset voltage of less than 500 mV. (As previously mentioned, this parameter may also be entered by specifying the upper and lower peak levels directly with the [UPR U] and [LWR V] keys instead of the [AMPL A] and [OFST D] keys.)

3.4.2.1.4 Burst Key

The [BRST R] key selects the number of waveform cycles that are generated when the generator is triggered in the BURST mode (mode 3). The burst count can be set from 1 to 1,048,200 cycles.

3.4.2.1.5 Function Key

The [FUNC C] key selects the type of waveform at the FUNC OUT connector.

[FUNC C] [0] selects a sine wave.

[FUNC C] [1] selects a triangle wave.

FUNC C 2 selects a square wave of the same polarity as the MAIN SYNC OUT signal.

FUNC C 3 selects a square wave of opposite polarity of the MAIN SYNC OUT signal.

FUNC C 4 selects the DC function. The FUNC OUT voltage is a DC level at the programmed OFFSET voltage. The AMPLITUDE and MODE settings have no effect on the output.

FUNC C 5 selects the EXTERNAL WIDTH function.

The FUNC OUT voltage is controlled by the AMPLITUDE, OFFSET and TRIGGER controls. For example, selecting amplitude 5V and offset 0V results in a FUNC OUT voltage of −2.5V when the generator is not triggered and +2.5V when triggered. Selecting amplitude 5V and offset 2.5V will result in an output voltage of 0V not triggered and 5V when triggered. The internal or external trigger gates the voltage to the high state for the duration of the trigger signal. With the following exception, the output will be gated by the trigger source regardless of the MODE programmed.

In the "burst" mode, (mode 3), the output will be gated to the high state for the duration of the burst count.

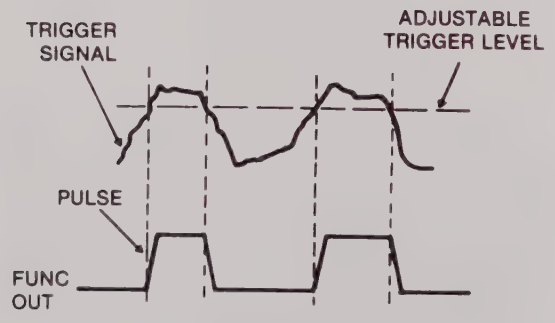


Figure 3-3. External Width

FUNC C 6 selects the SINGLE PULSE function. One pulse of programmable width will be produced for *each cycle* of the SYNC OUT signal. (For example, if the MODE is set to CONTINUOUS, pulses will be produced continuously.) Leading edge of pulse will coincide with positive-going transition of SYNC OUT signal.

FUNC C 7 selects the DELAY PULSE function. One pulse of programmable width will be produced for each cycle of SYNC OUT signal. Delay between leading edge of SYNC OUT signal and leading edge of pulse is programmable.

FUNC C 8 selects the DOUBLE PULSE function. Both the underlayed and delayed pulses will be produced (two pulses for each cycle of SYNC OUT signal).

3.4.2.1.6 Mode Key

The MODE B key determines the conditions under which the selected function will be present at the FUNC OUT connector.

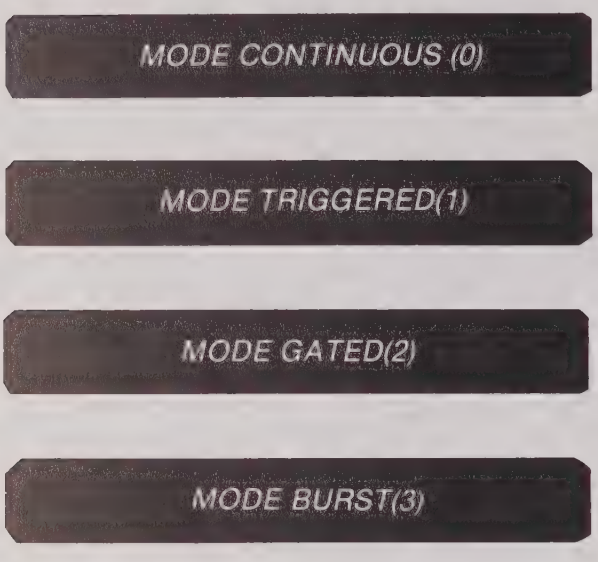
MODE B 0 selects a continuous waveform.

MODE B 1 selects a triggered waveform. One cycle of the selected function will be generated each time the generator is manually or externally triggered.

MODE B 2 selects a gated waveform. The selected function will be present at the FUNC OUT connector for the duration of the manual or external trigger signal. The last cycle started is completed.

MODE B 3 selects a the BURST mode. When the generator is manually or externally triggered, it will produce the number of waveform cycles previously programmed with the BRST R key.

The front panel displays for the various modes are:



3.4.2.2 Trigger Controls

The TRIG block of controls contains the parameter keys for external trigger slope, external trigger level (threshold), and manual trigger. The trigger keys affect the instrument output only in the TRIGGERED, GATED and BURST modes, or if the EXTERNAL WIDTH function has been selected.

3.4.2.2.1 Level Key

The [LVL XL] key selects the threshold level (in volts) for the external trigger signal applied to the TRIG IN connector.

3.4.2.2.2 Slope Key

The [SLP Q] key selects the external trigger slope. A parameter code of 0 selects positive trigger slope; a code of 1 selects negative trigger slope. Positive trigger slope causes the instrument to be triggered (in the triggered modes) as the external TRIG IN signal crosses the trigger threshold level in a positive-going direction, or to remain gated ON (in the gated modes) as long as the TRIG IN signal is more positive than the programmed threshold level. Negative trigger slope causes the instrument to be triggered as the TRIG IN signal crosses the trigger threshold level in a negative-going direction, or to remain gated ON as long as the TRIG IN signal is more negative than the programmed threshold level.

3.4.2.2.3 Manual Key

The [MAN J H] key manually triggers or gates the instrument when the key is pressed.

3.4.2.3 Pulse Controls

The PULSE control block contains the keys for pulse period, pulse delay, pulse width, upper and lower waveform voltage levels and pulse phase.

3.4.2.3.1 Pulse Period Key

The pulse [PER S] key is used to select pulse period (repetition time) in seconds. This key allows entry of generator frequency in terms of time (the reciprocal of frequency). It affects the frequency of square, triangle and sine waves as well as pulse period. Period range is 83.3 ns to 100 seconds.

3.4.2.3.2 Pulse Delay Key

The [DLY L] key is used to enter the desired pulse delay with respect to the SYNC OUT signal. This parameter is applicable only to the DELAY PULSE (7) function and the second pulse of the DOUBLE PULSE (8) function. Delay range is 80 ns to 100 ms. Delay may not be more than 50% of the programmed period if the delay is less than 500 ns. For delays of 500 ns or greater, the limit is 80% of period.

3.4.2.3.3 Pulse Width Key

The [WID N] key is used to enter the desired pulse width. It has no effect on sine, triangle or square waves. Width range is 40 ns to 100 ms. Width may not be more than 50% of the programmed period if the width is less than 500 ns. For widths of 500 ns or greater, the limit is 80% of period.

3.4.2.3.4 Upper and Lower Level Keys

The [UPR U] and [LWR V] keys are used to enter the desired upper and lower pulse voltage levels. Range is −5V to +5V. The upper level must always be programmed

to be more positive than the lower level. These are the voltages at the FUNC OUT connector when it is terminated with 50Ω. Open-circuit output voltages will be approximately twice as high. These keys are merely an alternate method of entering amplitude and offset, and effect sine, triangle and square waves as well as pulses. To avoid loss of amplitude resolution, amplitudes less than 100 mV require an offset voltage of less than 500 mV. For example, attempting to program an upper level of +5.00V and a lower level of +4.92V will result in display of the error message

AMPL/OFST CONFLICT

3.4.2.3.5 Pulse Complement Key

The [COMP] key selects either a normal (uninverted) or complement (inverted) pulse. [COMP] [0] selects a normal pulse; [COMP] [1] selects the pulse complement.

3.4.2.4 Stored Setting Controls

The SETTING block of controls contains two keys; [STOR M] and [RCL Y]. These keys are used to store instrument settings in non-volatile memory, and to recall user-stored and factory-programmed settings.

3.4.2.4.1 Store Key

The [STOR M] key causes the display to show the location of the settings most recently stored or deleted, and enables entry of a storage location for the current instrument settings. The settings stored are those in scratch-pad memory (whether they have been executed or not). Locations available for user-stored settings are 1 through 150. Entering a negative value (-1 through −150) deletes the settings at the specified storage location. An EXECUTE command is not required for storing a setting. The Wavetek 271 automatically stores the current instrument settings in location 0 when power is turned off.

3.4.2.4.2 Recall Key

The [RCL Y] key causes the display to show the location of the most recently recalled settings (if any), or the message resulting from previous recall of a factory-stored setting. Attempting to recall a message from a non-existent location will result in display of the error message

RECALL SETTING ERROR

A display of

CANNOT RECALL

indicates that the settings in that location have been deleted. An EXECUTE command is not required to recall settings to scratch-pad memory, but *is* required to transfer the settings from scratch-pad memory to waveform memory. Recall settings and selections are:

SETTINGS	RCL
Recall last power off condition	0
Recall user-stored settings	1-150
Internal calibration procedure	1000-1039
Internal QA test/demo procedure	2000-2009

Further information on the use of the stored settings may be found in section 3.4.6 of this manual.

3.4.2.5 Output Control

The OUT block of controls contains only one key, labelled [OUT ON P]. Entering a code of 0 turns the output off and leaves the output connector in a high-impedance state. A code of 1 turns the output on. A code of 2 turns the output off, but leaves the output connector terminated in approximately 50Ω.

3.4.2.6 GPIB Controls

The only parameter key in the GPIB block of controls is the [ADRS] key. (The [CMD RCL] and [LCL] keys were previously defined as action keys; that is, keys that

do not require a numerical parameter entry.) Pressing the [ADRS] key causes the GPIB address of the instrument to be displayed. At power-up, the GPIB address is always that of the internal switches. A new value of GPIB address may be entered from the keyboard if the internal disable switch has not been set. An EXECUTE command is not required. Pressing the [ADRS] key causes the [CMD RCL] key to display the characters "XA", but this code *cannot* be used to *remotely* change the GPIB address.

3.4.3 Numeric Keys

The numeric keys [0] through [9], [+/-], [.] and [EXP] are used to enter new parameter values. Data entry is free format (i.e., fixed point, floating point, or exponential (scientific) notation).

Fixed Point	Decimal point remains at far right.
Floating Point	You program the decimal point. It floats to the left in its designated position as you enter more numerals.
Exponential Notation	A value, [EXP] then followed by the exponent of a times ten multiplier. When the value (mantissa) is limited to one digit before the decimal point, exponential notation is called scientific notation.

Table 3-2 gives some examples of the many ways the value 100 can be programmed.

The digits entered before the [EXP] key is pressed are the mantissa; the digits entered after [EXP] (only two are allowed) are the exponent. The result is the mantissa times 10 to the exponent power. For example [9] [.] [9] [9] [EXP] [2] is equal to $9.99 \times 10^2 = 999$.

Only one decimal point and one [EXP] are allowed per number; additional ones are ignored. The sign toggle

Table 3-2. Examples of Value Programming

Local (Keyboard)	Remote (ASCII)	Standard Notation
100	100	100
0100	0100	100 (leading zeroes are ignored)
1 EXP 2	1E2	1×10^2
.01 EXP 4	.01E4	$.01 \times 10^4$
.01 EXP 304	.01E304	.01 X 10^4(last two exponent digits only are used)
1000 EXP ±1	1000E-1	1000×10^{-1}
1 EXP ±2±	1E-2-	1×10^2 (two minus signs cancel)
1 EXP .2	1E.2	1×10^2 (decimal points in exponent are ignored)

character [+/-] may appear any number of times. It causes the sign of the mantissa (if [EXP] has not been pressed) or the exponent (if [EXP] has been pressed) to be reversed (if negative, then positive, and vice versa) each time it appears. If an undesired value is entered prior to execution (the [EXEC] key), the [CLR] key can be used to erase it.

3.4.3.1 Parameter Termination and Execution

Because the number input format is so general, the microprocessor must be told when the last numeric character has been entered so it can evaluate the number. Numeric entry can be terminated by pressing any parameter key and some other command keys. In general, any key associated with an alphabetic

character (except [EXP] and [RST Z]) will terminate an entry.

When a numeric parameter entry is terminated, the new value is rounded off and tested to see if it is a legal value for the parameter being changed. If it is legal, the new value is entered into the instrument's scratch-pad memory. (See figure 3-2, Memory Structure.) Parameters are not transferred from scratch-pad memory to waveform circuit memory until the [EXP] key (or the cursor [↑] or [↓] keys) are pressed. An asterisk (*) in the display indicates that the parameter has been terminated but not yet executed, and may be erased before execution by using the [CLR] key. A few parameters that do not directly affect waveform circuit memory (such as GPIB [ADRS K] and SETTING [STOR M]) require only termination and not execution. These exceptions will be discussed separately.

3.4.3.2 Errors

Attempting to enter a value outside the legal limits of the parameter being programmed will result in an immediate error message when numeric entry is terminated. The instrument will disregard the new value and retain the previously programmed value in scratch-pad memory.

Example: Press [AMPL A] [1] [1] [AMPL A]. The display will indicate

```
AMPLITUDE ERROR
```

An error message is also displayed if a non-existent or deleted stored setting is recalled.

Interparameter inconsistencies (such as amplitude and offset that are individually within limits but add up to a peak output of greater than 5V peak into 50Ω) are not tested until the [EXEC I], [↑] or [↓] keys are pressed. The resulting error is displayed, and transfers of values are made to waveform circuits regardless of the error indicated.

Example: Press [AMPL A] [8] [OFST D] [4] [EXEC I]. The display will indicate

```
OUTPUT CLIPPING
```

3.4.4 Parameter Entry

Most parameters (commands that require a numeric entry) are entered first into scratch-pad memory, then transferred to waveform circuit memory when the [EXEC I] key is pressed. (See figure 3-2, Memory Structure.) This allows the instrument user to change all output waveform parameters simultaneously. A few parameters (such as GPIB [ADRS K] and [STOR M]) do not require an [EXEC I] command.

There are three basic methods of entering parameters:

1. Select the desired parameter, enter the desired numerical value or code, and execute the command. This causes an immediate parameter change.

   Example: [AMPL A] [1] [0] [EXP] [+/-] [3] [EXEC I]

   causes an immediate amplitude change to 10 mV.

2. Select the desired parameter, enter the desired numerical value or code, select the next parameter, enter the desired numerical value or code for this parameter, etc. After all parameter values have been entered, press [EXEC I] to change all parameters simultaneously.

   Example: [FUNC C] [2] [FUNC C] [FREQ F] [5] [EXP] [3] [MODE B] [0] [AMPL A] [1] [OUT ON P] [1] [EXEC I] results in a continuous 5 kHz square wave with peak-to-peak amplitude of 1V and turns on the generator output.

3. Select the desired parameter, then increment or decrement the present value with the [↑] or [↓] cursor controls. (This is particularly useful

for the MODE or FUNCTION parameters if you haven't yet learned their numerical codes, as the display will indicate both the parameter name and numerical code.)

For parameters that will accept more than one digit of numerical value, first select the digit to be incremented or decremented with the [←] and [→] cursor controls. The display will indicate the digit selected by alternately flashing this digit bright and dim. The [←] and [→] cursor keys have no effect on parameters which accept only a single digit, such as MODE or FUNCTION.

Note that use of the [↑] or [↓] cursor controls will cause an automatic EXECUTE and therefore an immediate change in the waveform parameter. If this is undesirable, the generator output may be temporarily turned off during parameter changes. (Press [OUT ON P] [0] [EXEC] or [OUT ON P] [↓].)

To continuously increment or decrement a parameter value, hold down the [↑] or [↓] cursor key.

The cursor controls will have no effect if the displayed parameter value is followed by a cursor in the form of a horizontal underline.

Example:

This indicates that entry of the value has already been started using the numeric keys, and that the instrument is expecting another numeric key, another parameter key, or the [CLR] or [EXEC] key.

To display the value of a parameter without changing it, press the parameter key but do not press any numeric keys or the [↑] or [↓] cursor keys. If the first character of the display is an asterisk, it indicates that the parameter has been entered only into scratch-pad memory, and not yet into waveform memory. An undesired entry in scratch-pad memory can be cleared with the [CLR] key.

Example: Press [AMPL A] [5] [EXEC]. The display will show

Press [AMPL A] [1] [AMPL A]. The display will now show

Press [CLR]. The display will return to

3.4.5 Stored Settings

User instrument settings may be stored in up to 150 internal memory locations, and later accessed either randomly or sequentially. In addition, the internal memory also contains an internal QA Test/Demonstration procedure and instrument settings used during the internal stored calibration procedure. Current instrument settings are automatically stored in location zero for retention when power is turned off.

3.4.5.1 Storage of Setting

To store an instrument setting, enter the desired parameters into scratch-pad memory. It is not necessary to transfer the parameters to waveform memory by pressing the [EXEC] key. Press the [STOR M] key, enter the number of the desired storage location (1 to 150), and press the [STOR M] key again.

Example: To store settings in memory location 25, press [STOR M] [2] [5] [STOR M]. The display will indicate

3.4.5.2 Deletion of Stored Setting

To delete a stored setting, press the STOR M key, the +/- key, and the number of the storage location to be deleted. Then press the STOR M key again.

Example: To delete stored setting 25, press STOR M +/- 2 5 STOR M. The display will indicate

No. 25 LAST DELETED

3.4.5.3 Recall of Stored Setting

To recall a stored setting, press the RCL Y key and the number of the setting to be recalled. Press the RCL Y key again to transfer the setting to scratch-pad memory, or press the EXEC I key to transfer the setting to waveform memory.

Examples:

To recall stored setting 3 to scratch-pad memory, press RCL Y 3 RCL Y .

To recall stored setting 3 to waveform memory, press RCL Y 3 EXEC I .

In either case, the display will indicate

No. 3 LAST RECALLED

Attempting to recall a deleted setting will result in a display of

CANNOT RECALL

3.4.5.4 Modification of Stored Setting

To modify a stored setting, recall the setting to scratch-pad memory, enter new value(s) for the parameter(s) to be changed, then store the setting back in the previous location.

Example: To change the amplitude parameter in stored setting #3 to 5V, press RCL Y 3 AMPL A 5 STOR M 3 STOR M .

3.4.5.5 Recall of Consecutive Stored Settings

To recall consecutive stored settings, recall and execute the first stored setting. Then use the cursor ↑ key to recall the next higher-numbered stored setting, or the ↓ key to recall the next lower-numbered stored setting. Using the cursor keys causes an automatic EXECUTE, and also causes deleted settings to be skipped.

Example:

KEYSTROKES	DISPLAY AFTER KEYSTROKES
RCL Y 1 0 EXEC I	No. 10 LAST RECALLED
↑	No. 11 LAST RECALLED
↑	No. 12 LAST RECALLED

3.4.5.6 Recall of Last Power Off Condition

To recall the last power-off condition of the instrument, press RCL Y 0 EXEC I . Note that this command must be used *immediately* after power-on, *before* any other command is executed. Memory #0 is constantly updated with instrument status at each press of the EXEC I key, and will no longer contain the previous power-off parameters after any other command is executed.

3.4.5.7 Stored Performance Verification

An internally stored program exercises the instrument circuits to enable a quick verification of operation. An oscilloscope must be used to observe this procedure. Connect as shown in Figure 3-4 and set up the scope as follows:

1. Trigger on sync output (CH2).
2. Set Time/Div to 0.5 mS.
3. Set CH1 to 2V/Div.
4. Set CH2 to 2V/Div.

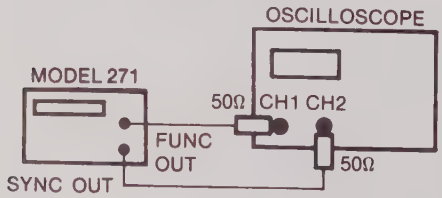


Figure 3-4. Test Connections for Stored Performance Verification

Press [RCL Y] [2] [0] [0] [0] [EXEC ↑] to start the Quality Assurance procedure. The display will indicate

(0) BEGIN QA PROC

The oscilloscope displays a function output sine wave and a sync output square wave.

Press [↑] to select these steps:

1. A sweep from 1 kHz to 10 kHz.
2. A rapid stepping of amplitude.
3. A square wave that steps from a negative to positive offset and repeats.
4. A pulse delay test.
5. A pulse width test.
6. A trigger test.
7. A gate test.
8. A burst test.
9. End QA procedure.

These tests are explained in greater detail in Table 2-3, Initial Checkout, in the Installation and Interface section of the manual.

3.4.5.8 Calibration Procedure

The calibration procedure is called by pressing [RCL Y] [1] [0] [0] [0] [RCL Y]. The front panel display will read "(0) CAL 271 (VX.Y)" where X.Y identifies the software version. Each press of [↑] steps to the next calibration prompt. Press [↑] and observe the display:

(1) + 15V SUPP, R39

This display tells the technician to adjust the +15V power supply with potentiometer R39. By pressing [↑], all calibration prompts can be displayed and required internal control setups will be made automatically. Test points and test equipment setup are included in section 5 of the manual.

3.4.6 VCG Operation

The frequency of the Wavetek 271 may be controlled by an ac or dc signal applied to the VCG IN BNC connector. A positive control voltage will increase the generator frequency; a negative voltage will decrease frequency. Frequency may be changed by the VCG control voltage only within a frequency range. Table 3-3, Internally Selected Frequency Ranges, shows the frequency ranges corresponding VCG ranges. Figure 3-5, VCG (FM) Nomograph, illustrates the VCG voltage required to change the programmed frequency to the desired output frequency. (Frequencies in this figure are shown as significant digits, without the range multiplier.) Frequency range must be selected before applying the VCG signal.

For example, Table 3-3 shows that if the frequency is programmed to 500 Hz, the Wavetek 271 selects the 10^2 range. As shown in the example of Figure 3-5, a programmed frequency of 500 Hz and a +5V VCG input will produce an actual output frequency of 1 kHz.

Another example is a 1200:1 frequency sweep from 1 kHz to 1.2 MHz using 0.01 to 12.0 volt VCG signal. Table 3-3 shows that the frequency range is 10^5. To get in that range, program any value within the 10^5

Table 3-3. Internally Selected Frequency Ranges

Range Name	Programmed Frequency Range	VCG Range	Percent Frequency (XF) Range (GPIB Only)
10^6	1.00 MHz-12.0 MHz	10.0 kHz-12.0 MHz	0-10 MHz
10^5	100 kHz-999 kHz	1.00 kHz-1.20 Mhz	0-1.00 MHz
10^4	10.0 kHz-99.9 kHz	100 Hz-120 kHz	0-100 kHz
10^3	1.00 kHz-9.99 kHz	10.0 Hz-12.0 kHz	0-10 kHz
10^2	100 Hz-999 Hz	1.00 Hz-1.20 kHz	0-1.00 kHz
10^1	10.0 Hz-99.9 Hz	100 mHz-120 Hz	0-100 Hz
10^0	1.00 Hz-9.99 Hz	10 mHz-12.0 Hz	0-10.0 Hz
10^{-1}	100 mHz-999 mHz	1.00 mHz-1.20 Hz	0-1.00 Hz
10^{-2}	10.0 mHz-99.9 mHz	100 μHz-120 mHz	0-100 mHz

range. Next, program [FREQ F] [0] [EXEC I]. The display will show

(This will leave the generator set to the desired range, but remove the internally generated frequency control voltage.) A 0.01 volt VCG voltage will cause the output frequency to be 1 kHz, and a 0.01V to 12V VCG input will cause a 1 kHz to 1.2 MHz frequency sweep.

3.4.7 Percent Frequency (XF)Command

Percent of frequency (0 to 100% in 0.1% increments) within any given range may be remotely programmed via the GPIB by using the ASCII control code "XF". (This command is not available from the front panel keyboard.) Before the Percent Frequency (XF) command may be used, the generator must first be set to the desired range by programming any frequency within that range. (Frequency ranges are shown in table 3-3.) Note that on the highest range, the maximum frequency that may be programmed by using the XF command is 10.0 MHz.

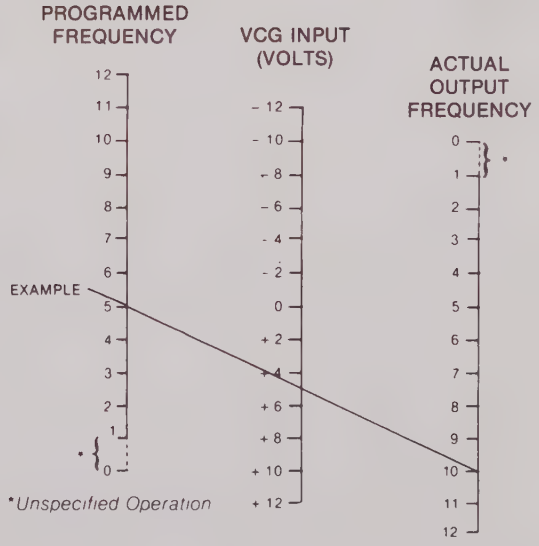


Figure 3-5. VCG (FM) Nomograph

3.5 REMOTE OPERATION

The Wavetek 271 may be remotely controlled via the General Purpose Interface Bus (GPIB). To remotely control the instrument:

1. Connect the instrument to the GPIB system with the standard GPIB connector. (See section 2.2.3 of the manual.)
2. Set the instrument GPIB address to a unique device identification number (between 0 and 30) either with the internal switches or with the front panel GPIB ADRS key. (See section 2.2.4 of the manual.)
3. Remotely program the desired instrument GET, SRQ and Talk responses by sending the XG, XQ and XT codes along with the proper numerical value for each parameter. (The exact method of sending the characters will depend on the type of controller being used.)
4. Send the desired ASCII control codes over the GPIB to the instrument.

3.5.1 ASCII Control Codes

The remote control ASCII characters for the Wavetek 271 are listed in Appendix B, Programming Command Summary. Please note that:

1. Not all front panel keys have a directly equivalent remote control command. These keys are:
   The cursor keys ↑ ↓ ← →
   CLR
   ♪
   DISP TEST
   STAT
   SRQ
   GPIB ADRS
   CMD RCL
   LCL
2. Not all remote control commands have a directly equivalent front panel key. These commands are:
   Percent Frequency (XF)
   GET mode (XG)
   SRQ Mode (XQ)
   Talk Mode (XT)
   Recall Next Lesser Numbered Program (XU)
   Terminator (XV)
   Recall Next Greater Numbered Program (XW)
3. In most cases, the front panel keys that have an equivalent remote control command are marked with the corresponding ASCII control codes. The exception is EXP.
4. Some of the remote control commands consist of two letters, and start with the letter "X". This letter "X" is merely a prefix that is used in order to allow the number of remote control codes to exceed the number of letters in the alphabet. These two-letter codes must be sent without any space, punctuation or other character between the letters.
5. One front panel key performs two functions, but has separate remote control codes for each function. This key is MAN trigger (J gates on, H gates off).

3.5.2 Setting Instrument GET, SRQ and Talk Modes

3.5.2.1 Setting the Talk Mode

The Talk mode determines what the instrument will say when it is addressed as a talker on the GPIB. The talk mode is remotely programmed with the XT command. Valid parameter values are XT0 through XT8. Only one talk response may be programmed at any one time.

XT0 Programming error list (only errors from GPIB input). XT0 is the power-up talk mode. A typical error string is E 1F 2AD 3Y. Some error string characteristics are:

a. All error strings begin with E.
b. Most recent error is at the end of string.
c. Errors are separated by blanks.
d. Class 1 errors: A 1 followed by programming character that caused the error.
e. Class 2 errors: A 2 followed by the two conflicting program characters.
f. Class 3 errors: A 3 followed by M (store) or Y (recall).
g. Error strings can be up to 80 characters including E and blanks.
h. After transfer, the instrument clears the error string.

XT1 Poll Byte Response. The byte that would be sent if a serial poll were to be performed. The controller, upon reading this byte, clears the poll byte and resets the SRQ line if asserted.

XT2 The most recently selected parameter and its value. Example: FREQ 1E3. (The "most recently selected parameter" is the parameter at the end of the command string.) If no parameter is selected; e.g., power-on state, reset, or execute command, then the instrument returns NO PARAMETER SELECTED. Note that the NO PARAMETER SELECTED message will be returned if the last command in the string is an EXECUTE command (I).

XT3 The entire instrument setup after last execute. Example: F1E3A1D0C0P0Q0XL1.5.

XT4 The instrument setup when execute is received; the same format as XT3.

XT5 Instrument Identification: WAVETEK MODEL 271 V(X.Y). X.Y identifies the software version number.

XT6 The time since the instrument was powered on. Example: TIME: 1.3. Unit of measure is hours with 0.1 hour (6 minute) resolution.

XT7 The accumulated operating time. Example: TOTAL TIME: 306.2.
NOTE: Toggling switch 7 (figure 2-2) clears the instrument operating-time clock. With SW7 on, the clock runs during power on. With SW7 off, the clock clears to zero.

XT8 The number of stored settings installed. For the Wavetek 271: STORED SETTINGS 150.

3.5.2.2 Setting the SRQ Mode

The SRQ mode determines the conditions under which the instrument will send a service request message (SRQ) to the controller. Unlike the Talk mode, which allows only one response at a time to be programmed, the SRQ mode may be programmed for any desired combination of conditions.

XQ followed by a value (0 through 255) selects the conditions under which the Wavetek 271 asserts the SRQ line and rsv (request for service) bit. The equivalent binary value is a "mask" for the serial poll response byte (shown in table 3-4). The binary mask selects certain conditions that will be recognized as conditions that assert the SRQ line and rsv bit. All other conditions are ignored (masked).

Table 3-4 shows the serial poll response byte. Each of the 8 bits represents a condition that, if selected by the SRQ mode, will assert the GPIB's SRQ line and the serial poll byte's rsv bit. Each bit may be selected individually or in various combinations. The rsv bit (bit decimal value 64) will have no effect if selected.

For example, XQ1 dictates that the SRQ line and the serial poll byte's rsv bit are asserted when there is a program error; such as a frequency beyond the instrument's limits. The serial poll response byte will be 0100 0001.

In another example, XQ131 dictates that the SRQ line and the rsv bit are asserted when a program error has occurred, the output protection is enabled, or the SRQ key is pressed. The serial poll response byte will be 1100 0011.

Table 3-4. Serial Poll Response Byte

Bit Binary Position	Bit Decimal Value	Bit Name	Bit Description
1000 0000	128 (MSB)	SRQ Key	Indicates that front panel SRQ key has been pressed.
0100 0000	64	rsv	Request for Service.
0010 0000	32	Undefined	Undefined bit..
0001 0000	16	Undefined	Undefined bit.
0000 1000	8	Low Battery	Indicates a low battery level for memory back-up battery.
0000 0100	4	Fuse Blown	Indicates output connector fuse has blown.
0000 0010	2	Output Protection	Indicates output protection is tripped.
0000 0001	1 (LSB)	Program Error	Indicates a program error.

To select the SRQ mode:

1. Determine the conditions under which you want the instrument to sent an SRQ message to the controller.
2. Look up (in table 3-4) the decimal value of the serial poll response bit that corresponds to each desired condition.
3. Add the decimal values of the selected bits.
4. Program the instrument with the XQ code and this decimal value.

3.5.2.3 Setting the GET Mode

XG followed by its code selects what actions occur when a Group Execute Trigger (GET) command is sent to the Wavetek 271. This code may be 0, 1 or −1.

Programmed Code	Instrument Response
0	Upon receipt of the GET, the programmed waveform values are transferred to the waveform generator circuits, and then the microprocessor sends a trigger pulse if the mode is not continuous. This is the same sequence of events that would occur if an execute, then a trigger action (IJH) were programmed, except that no error checking is done. GET mode 0 is the power-up condition.
1	Upon receipt of GET, the stored setting next in sequence after the last stored setting accessed is recalled, if it exists. Then the actions described for code 0 are performed. This is the same sequence of events that would occur if a next setting, an execute and a trigger action (XWIJH) were programmed, except that no error checking is done.
−1	Upon receipt of GET, the stored setting previous in sequence before the last stored setting accessed is recalled if it exists. Then the actions described for code 0 are performed. This is the same sequence of events that would occur if a previous setting, an execute and a trigger action (XUIJH) were programmed, except that no error checking is done.

3.5.3 Setting the End of String (Terminator) Character

XV followed by its argument designates a new End Of String (EOS) or terminator character. The argument is the decimal value of the ASCII character that is to be the new terminator (the EOS character recognized by the Wavetek 271). Any ASCII character except NUL is accepted.

The terminator character has two uses. During output, it is appended to the end of every response to a talk request on the GPIB. During input, it signals the end of a group of programming characters. Since it is always recognized, even in a quoted string, it can be used to ensure that the instrument is in a known state, so that following programming characters will be interpreted correctly.

At power-on time, the EOS character is the line feed control character, ASCII character LF (decimal value 10). When the Wavetek 271 issues a talk message, the EOS character is the last byte sent. In addition, the End Or Identify (EOI) line is pulsed low (END message) during the EOS character transmission. If the GPIB controller does not look for the END message (EOI line low), and it does not recognize the Line Feed (LF) as a string terminator, a new EOS character will be needed. For example, to change the EOS character from an LF to a Carriage Return (CR), program XV13. (Numerical values of ASCII characters are listed in Appendix A.)

3.5.4 Remote Control of Instrument Display

The single quote character (') is used to program a string of characters to be displayed on the front panel display. Program a single quote, the characters to be displayed, followed by either another single quote or by the terminator character. When the second quote or the terminator is programmed, the first 20 characters programmed after the first quote are displayed on the front panel. If fewer than 20 characters are programmed, then blanks are added to fill the display.

3.5.5 Differences Between Controllers

GPIB control commands are *not* part of the standardized BASIC computer language, and will vary from one make of controller to the next. For example, the Wavetek 6000 Instrumentation Computer uses a WRITE statement to send information to the instrument, while another make uses an OUTPUT command. Obviously, you will have to consult your controller manual for the proper controller commands. The GPIB commands and sample programs in this

manual were written using a Wavetek 6000 Instrumentation Computer, with the Wavetek 271 GPIB address set to 09.

3.5.6 Sending Instrument Commands

To send GPIB commands to the Wavetek 271 it is not necessary to individually control the GPIB lines or send bus management commands such as "attention" or "unlisten". The controller handles this chore automatically. For example, to set the instrument output amplitude to 5V, the command is WRITE @709:"A5I". This command sends the ASCII characters "A5I" via interface 7 to instrument 09. Alphabetic characters must be sent enclosed in quotation marks or as an alphanumeric variable. Numeric characters may also be sent as a numeric value or a numeric variable. For example, if the numeric variable X contains the value 5 and alphanumeric variable Y$ contains the ASCII characters A5I, then the following commands are all equivalent:

```
WRITE @709:"A5I"
WRITE @709:"A",5,"I"
WRITE @709:"A",X,"I"
WRITE @709:Y$
```

3.5.7 Reading Instrument Responses

Except for asserting the SRQ line, the instrument will not transmit data on the bus until it is commanded to do so by the controller. The two ways that the controller requests information are with a talk command or a serial poll. (The Wavetek 271 does not use the parallel poll.)

3.5.7.1 Talk Command

The controller we are using in these examples uses a READ statement to command the instrument to talk. The instrument response is read into an alphanumeric variable, then the variable is displayed on the controller screen. *What* the instrument will say when it is addressed to talk depends on the talk message (XT) code previously programmed. The commands used are:

Program Statements	Explanation
READ @709:READBACK$	Command instrument on interface 7 address 9 to talk. Place received data in alphanumeric variable READBACK$. Note that the Wavetek 6000 Instrumentation Computer allows variable names of unlimited length.
WRITE @0:READBACK$	Display contents of alphanumeric variable READBACK$ on controller screen.

3.5.7.2 Serial Poll

A serial poll is usually performed after one of the instruments on the bus asserts the SRQ line. It is done to determine *which* instrument originated the SRQ, and *what* the the problem (or condition) is. The serial poll response byte is read into a numeric variable. The numeric value of the variable may be printed or displayed, or the bits in the variable can be individually checked and a predetermined action taken. The conditions that will cause the SRQ line to be asserted depend on the previously programmed value of the SRQ (XQ) code.

Example 1:

Program Statements	Explanation
STATUS @709:DEVICE__STATUS	Read the status byte of device 09 (Wavetek 271) on port 7 (GPIB). Place results in numeric variable DEVICE__STATUS. Note that the Wavetek 6000 Instrumentation computer allows the use of the underscore character in the variable name, but not a space.
WRITE @0:"DEVICE STATUS = "; DEVICE__STATUS	Display value of numeric variable DEVICE__STATUS on controller screen.

Example 2:

Program Statements	Explanation
STATUS @709:STATUS_BYTE	Read the status byte of device 09 (Wavetek 271) on port 7 (GPIB). Place results in numeric variable DEVICE_STATUS.
IF BIT(0,STATUS_BYTE) THEN WRITE @0:"PROGRAM ERROR"	If bit 0 of numeric variable STATUS_BYTE is equal to 1 then display "PROGRAM ERROR" message on controller screen.
IF BIT(1,STATUS_BYTE) THEN WRITE @0:"OUTPUT PROTECTION"	If bit 1 of numeric variable STATUS_BYTE is equal to 1 then display "OUTPUT PROTECTION" message on controller screen.
IF BIT(2,STATUS_BYTE) THEN WRITE @0:"FUSE BLOWN"	If bit 2 of numeric variable STATUS_BYTE is equal to 1 then display "FUSE BLOWN" message on controller screen.
IF BIT(3,STATUS_BYTE) THEN WRITE @0:"LOW BATTERY"	If bit 3 of numeric variable STATUS_BYTE is equal to 1 then display "LOW BATTERY" message on controller screen.
IF BIT(7,STATUS_BYTE) THEN WRITE @0:"FRONT PANEL SRQ KEY PRESSED"	If bit 7 of numeric variable STATUS_BYTE is equal to 1 then display "FRONT PANEL SRQ KEY PRESSED" message on controller screen.

Note that in the above example that we did not check the condition of bit 6 in the serial poll response byte. This is the "request for service" bit, and will automatically be 1 if any of the other bits are 1. However, in a large system with many instruments on the bus, it may be desirable to first check bit 6 to determine which instrument(s) are requesting service, then check the remaining bits to determine what services the instrument is requesting.

3.5.8 SRQ Interrupts

The method of handling SRQ interrupts is highly dependent on the type of controller. For the controller used for the sample demonstration programs in this manual, SRQ interrupts are handled by interrogating the GPIB registers and storing the value in a numeric variable. Bit 10 in this numeric variable, which corresponds to the status of the SRQ line, is then checked to see if the bit value is 1. If so, a serial poll is then performed to determine which instrument(s) requested service.

The following example is from the sample demonstration programs in this manual:

Example:

Program Statements	Explanation
• • •	
170 GO SUB CHECK__FOR__SRQ	Perform subroutine labelled CHECK__FOR__SRQ to check for an interrupt.
• • •	
260 CHECK__FOR__SRQ: ASK @7:GPIB__REGISTERS	Label for subroutine to check SRQ line. Retrieve the contents of both the bus register and status register from the I/O card of GPIB port 7. Place the results in numeric variable GPIB__REGISTERS.
• • •	
270 IF BIT(10,GPIB__REGISTERS) THEN GO SUB SERIAL__POLL	Check the value of bit 10 (SRQ line) in numeric variable GPIB__REGISTERS. If the bit value is 1 then perform the subroutine labelled SERIAL__POLL.
• • •	

Statement 170 sends the program to the subroutine labelled CHECK__FOR__SRQ.

Statement 260 copies the contents of the GPIB registers into numeric variable GPIB__REGISTERS.

Statement 270 checks bit 10 in the numeric variable GPIB__REGISTERS, and if it is equal to 1 sends the program to the subroutine labelled SERIAL__POLL.

Once again, the reader is reminded that the sample programs and statements in this manual were written using one particular make of controller, and that it will be necessary for the user to check the programming manual for his controller.

3.5.9 Sample Demonstration Programs

Because each test system is unique and controller programming commands are not standardized, it is impossible to provide actual application programs in this manual. The following sample demonstration programs were written for a Wavetek 6000 Instrumentation Computer controlling a single instrument (the Wavetek 271), and demonstrate instrument control, readback from instrument, SRQ interrupts and the serial poll. The programs also demonstrate some of the Wavetek extensions of the BASIC computer language: Program labels, DO loops, and unlimited length variable names. In all programs the controller GPIB port is interface #7, and the Wavetek 271 GPIB address is set to 9. The programs are presented as tables containing both the actual program statements and explanatory comments.

Table 3-5 contains a simple program to send control commands to the Wavetek 271 and read back the instrument response. It does not monitor the SRQ line nor perform a serial poll.

Table 3-5. Sample Demonstration Program 271-1

Program Statements	Explanation
100 ! PROGRAM 271-1	Comment statement containing program identification.
110 DIM CONTROL$*80	Set length of alphanumeric control variable for maximum expected number of control characters.
120 DIM READBACK$*80	Set length of alphanumeric readback variable for maximum expected number of readback characters.
130 CLEAR	Clear controller screen.
140 DO	Start of endless loop. (No UNTIL or WHILE condition is specified.)
150 WRITE @0:"ENTER ASCII CONTROL CODES."	Prompt user for control codes.
160 INPUT CONTROL$	Stop program while user types instrument control codes into controller, then place control codes into alphanumeric variable CONTROL$.
170 WRITE @709:CONTROL$	Send control codes in alphanumeric variable CONTROL$ via interface 7 (GPIB) to instrument with GPIB address 9 (Wavetek 271).
180 READ @709:READBACK$	Command instrument on interface 7 address 9 to talk. Place received data in alphanumeric variable READBACK$.
190 WRITE @0:READBACK$	Display contents of alphanumeric variable READBACK$ on controller screen.
200 LOOP	End of loop. Return to DO statement to prompt user for next instrument control codes.
210 END	End of program.

Table 3-6 contains a slightly more elaborate program to send control commands to the Wavetek 271 and read back the instrument response. It does not monitor the SRQ line, but does perform a serial poll and display the results as a numerical value.

Table 3-6. Sample Demonstration Program 271-2

Program Statements	Explanation
100 ! PROGRAM 271-2	Comment statement containing program identification.
110 DIM CONTROL$*80	Set length of alphanumeric control variable for maximum expected number of control characters.
120 DIM READBACK$*80	Set length of alphanumeric readback variable for maximum expected number of readback characters.
130 CLEAR	Clear controller screen.
140 DO	Start of endless loop. (No UNTIL or WHILE condition is specified.)
150 WRITE @0:"ENTER ASCII CONTROL CODES."	Prompt user for control codes.
160 INPUT CONTROL$	Stop program while user types instrument control codes into controller, then place control codes into alphanumeric variable CONTROL$.
170 WRITE @709:CONTROL$	Send control codes in alphanumeric variable CONTROL$ via interface 7 (GPIB) to instrument with GPIB address 9 (Wavetek 271).
180 READ @709:READBACK$	Command instrument on interface 7 address 9 to talk. Place received data in alphanumeric variable READBACK$.
190 WRITE @0:READBACK$	Display contents of alphanumeric variable READBACK$ on controller screen.
200 STATUS @709:DEVICE_STATUS	Read the status byte of device 09 (Wavetek 271) on port 7 (GPIB). Place results in numeric variable DEVICE_STATUS.
210 WRITE @0:"DEVICE STATUS = "; DEVICE_STATUS	Display value of numeric variable DEVICE_STATUS on controller screen.
220 LOOP	End of loop. Return to DO statement to prompt user for next instrument control codes.
230 END	End of program.

Table 3-7 contains a program to send control commands to the Wavetek 271, read back the instrument response, monitor the SRQ line, perform a serial poll and display the results as a message on the controller screen. Because the program stops at the INPUT statement, it does *not* monitor for a *delayed* SRQ, such as "FUSE BLOWN".

Table 3-7. Sample Demonstration Program 271-3

Program Statements	Explanation
100 ! PROGRAM 271-3	Comment statement containing program identification.
110 DIM CONTROL$*80	Set length of alphanumeric control variable for maximum expected number of control characters.
120 DIM READBACK$*80	Set length of alphanumeric readback variable for maximum expected number of readback characters.
130 CLEAR	Clear controller screen.
140 DO	Start of endless loop (no UNTIL or WHILE condition is specified).
150 WRITE @0:"ENTER ASCII CONTROL CODES."	Prompt user for control codes.
160 INPUT CONTROL$	Stop program while user types instrument control codes into controller, then place control codes into alphanumeric variable CONTROL$.
170 WRITE @709:CONTROL$	Send control codes in alphanumeric variable CONTROL$ via interface 7 (GPIB) to instrument with GPIB address 9 (Wavetek 271).
180 READ @709:READBACK$	Command instrument on interface 7 address 9 to talk. Place received data in alphanumeric variable READBACK$.
190 WRITE @0:READBACK$	Display contents of alphanumeric variable READBACK$ on controller screen.
200 ASK @7:GPIB_REGISTERS	Retrieve the contents of both the bus register and status register from the I/O card of GPIB port 7. Place the results in numeric variable GPIB_REGISTERS.
210 IF BIT(10,GPIB_REGISTERS) THEN GO SUB SERIAL_POLL	Check the value of bit 10 (SRQ line) in numeric variable GPIB_REGISTERS. If the bit value is 1 then perform the subroutine labelled SERIAL_POLL.
220 LOOP	End of loop. Return to DO statement to prompt user for next instrument control codes.
230 SERIAL_POLL:STATUS @709:STATUS_BYTE	Program label indicating start of serial poll subroutine. Perform serial poll of instrument on interface 7 (GPIB) address 9. Place results in numeric variable STATUS_BYTE.
240 IF BIT(0,STATUS_BYTE) THEN WRITE @0:"PROGRAM ERROR"	If bit 0 of numeric variable STATUS_BYTE is equal to 1 then display "PROGRAM ERROR" message on controller screen

Table 3-7. Sample Demonstration Program 271-3 (Continued)

Program Statements	Explanation
250 IF BIT(1,STATUS_BYTE) THEN WRITE @0:"OUTPUT PROTECTION"	If bit 1 of numeric variable STATUS_BYTE is equal to 1 then display "OUTPUT PROTECTION" message on controller screen.
260 IF BIT(2,STATUS_BYTE) THEN WRITE @0:"FUSE BLOWN"	If bit 2 of numeric variable STATUS_BYTE is equal to 1 then display "FUSE BLOWN" message on controller screen.
270 IF BIT(3,STATUS_BYTE) THEN WRITE @0:"LOW BATTERY"	If bit 3 of numeric variable STATUS_BYTE is equal to 1 then display "LOW BATTERY" message on controller screen.
280 IF BIT(7,STATUS_BYTE) THEN WRITE @0:"FRONT PANEL SRQ KEY PRESSED"	If bit 7 of numeric variable STATUS_BYTE is equal to 1 then display "FRONT PANEL SRQ KEY PRESSED" message on controller screen.
290 RETURN	End of serial poll subroutine.
300 END	End of program.

Table 3-8 contains a program to send control commands to the Wavetek 271, read back the instrument response, monitor the SRQ line, perform a serial poll and display the results as a message on the controller screen. This program continuously monitors for a delayed SRQ, such as "FUSE BLOWN".

Table 3-8. Sample Demonstration Program 271-4

Program Statements	Explanation
100 ! PROGRAM 271-4	Comment statement containing program identification.
110 DIM CONTROL$*80	Set length of alphanumeric control variable for maximum expected number of control characters.
120 DIM READBACK$*80	Set length of alphanumeric readback variable for maximum expected number of readback characters.
130 CLEAR	Clear controller screen.
140 WRITE @0:"ENTER ASCII CONTROL CODES."	Prompt user for control codes.
150 INPUT CONTROL$	Stop program while user types instrument control codes into controller, then place control codes into alphanumeric variable CONTROL$.
160 WRITE @709:CONTROL$	Send control codes in alphanumeric variable CONTROL$ via interface 7 (GPIB) to instrument with GPIB address 9 (Wavetek 271).
170 GO SUB CHECK_FOR_SRQ	Perform subroutine labeled CHECK_FOR_SRQ to check for an interrupt.

Table 3-8. Sample Demonstration Program 271-4 (Continued)

Program Statements	Explanation
180 READ @709:READBACK$	Command instrument on interface 7 address 9 to talk. Place received data in alphanumeric variable READBACK$.
190 WRITE @0:READBACK$	Display contents of alphanumeric variable READBACK$ on controller screen.
200 WRITE @0	Display blank line on controller screen.
210 WRITE @0:"PRESS 'STOP' AND 'RUN' KEYS TO ENTER NEW COMMAND."	Display message to prompt operator to stop then restart program to enter new command.
220 WRITE @0	Display blank line on controller screen.
230 DO	Start of endless loop (no UNTIL or WHILE condition is specified) to check for SRQ interrupt.
240 GO SUB CHECK__FOR__SRQ	Perform subroutine labeled CHECK__FOR__SRQ to check for an interrupt.
250 LOOP	End of loop to continuously check for SRQ interrupt.
260 CHECK__FOR__SRQ:ASK @7:GPIB__REGISTERS	Label for subroutine to check SRQ line. Retrieve the contents of both the bus register and status register from the I/O card of GPIB port 7. Place the results in numeric variable GPIB__REGISTERS.
270 IF BIT(10,GPIB__REGISTERS) THEN GO SUB SERIAL__POLL	Check the value of bit 10 (SRQ line) in numeric variable GPIB__REGISTERS. If the bit value is 1 then perform the subroutine labelled SERIAL__POLL.
280 RETURN	End of subroutine to check for SRQ interrupt.
290 SERIAL__POLL:STATUS @709:STATUS__BYTE	Program label indicating start of serial poll subroutine. Perform serial poll of instrument on interface 7 (GPIB) address 9. Place results in numeric variable STATUS__BYTE.
300 IF BIT(0,STATUS__BYTE) THEN WRITE @0:"PROGRAM ERROR"	If bit 0 of numeric variable STATUS__BYTE is equal to 1 then display "PROGRAM ERROR" message on controller screen.
310 IF BIT(1,STATUS__BYTE) THEN WRITE @0:"OUTPUT PROTECTION"	If bit 1 of numeric variable STATUS__BYTE is equal to 1 then display "OUTPUT PROTECTION" message on controller screen.
320 IF BIT(2,STATUS__BYTE) THEN WRITE @0:"FUSE BLOWN"	If bit 2 of numeric variable STATUS__BYTE is equal to 1 then display "FUSE BLOWN" message on controller screen.

Table 3-8. Sample Demonstration Program 271-4 (Continued)

Program Statements	Explanation
330 IF BIT(3,STATUS_BYTE) THEN WRITE @0:"LOW BATTERY"	If bit 3 of numeric variable STATUS_BYTE is equal to 1 then display "LOW BATTERY" message on controller screen.
340 IF BIT(7,STATUS_BYTE) THEN WRITE @0:"FRONT PANEL SRQ KEY PRESSED"	If bit 7 of numeric variable STATUS_BYTE is equal to 1 then display "FRONT PANEL" SRQ KEY PRESSED" message on controller screen.
350 RETURN	End of serial poll subroutine.
360 END	End of program.

3.6 THE GENERAL PURPOSE INTERFACE BUS

This section of the manual is provided for readers who wish further background information on the GPIB.

The GPIB interface in the Wavetek 271 is an implementation of the IEEE 488-1978 standard as a computer-to-peripheral and a peripheral-to-peripheral interface. This implementation includes all electrical, mechanical, timing and protocol considerations. It supports the following interface functions:

SH1 Complete source handshake.
AH1 Complete acceptor handshake.
T6 Basic Talker.
TE0 No extended talker.
L4 Basic listener.
SR1 Complete service request (software select).
RL1 Remote/local and local lockout.
PP0 No parallel poll capability.
DC1 Complete device clear/selective device clear.
DT1 Complete device trigger capability.
E2 Tri-state drivers.

The talk capability allows a device to send data (such as error message readings) out over the bus. The listen capability allows a device to receive data (such as device programming information) from the bus.

3.6.1 GPIB Structure

The General Purpose Interface Bus consists of 16 negative-true signal lines as shown in Figure 3-6. These 16 lines include 8 bi-directional data lines, 3 handshake lines and 5 control lines. All devices on the bus interface to these lines with passive pull-up and active pull-down. Thus, any device may "assert" a line by pulling it down to the logic low, or "true" state. If no device is asserting the line, it is pulled up to the logic high, or "false" state. (Only the controller is allowed to assert certain lines.)

As shown in Figure 3-6, devices connected to the bus may be a LISTENER (only), TALKER (only), LISTENER/TALKER or CONTROLLER. More than one controller may be connected to the bus, but only one controller may be hard-wired as SYSTEM CONTROLLER, and only one controller at a time may assume the role of ACTIVE CONTROLLER.

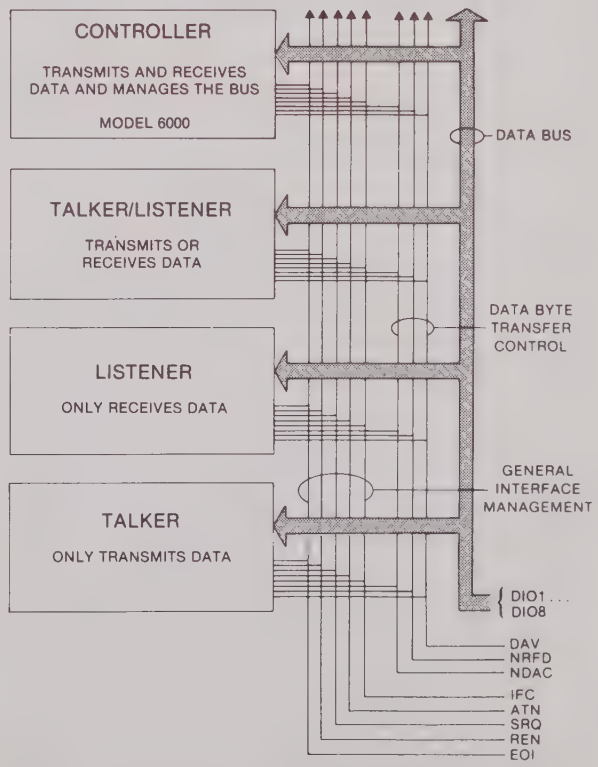


Figure 3-6. GPIB Structure

3.6.2 GPIB Lines

The mnemonics used to identify the GPIB lines are:

DIO1-DIO8	Data In/Out Lines
ATN	Attention
REN	Remote Enable
DAV	Data Available
NRFD	Not Ready For Data
NDAC	Not Data Accepted
EOI	End Or Identify
SRQ	Service Request
IFC	Interface Clear

The functions of the GPIB lines are:

DIO1-DIO8 These eight lines (Data In/Out) are used to send commands from the controller and to transfer data back and forth between instruments and the controller.

ATN The Attention line is operated only by the active controller. It specifies whether the information on lines DIO1-DIO8 is data (ATN false) or a command (ATN true). Whenever ATN is set true, no activity is allowed on the bus except for controller-originated messages.

REN The Remote Enable line controls whether devices on the GPIB are in local or remote modes. In the local mode, devices respond to front panel commands and do not respond to GPIB originated commands. In remote mode, the situation is reversed; GPIB originated commands are obeyed, while front panel commands are ignored. The Wavetek 271 enters the remote state when it receives its listen address and REN is enabled. The Wavetek 271 then stays in the remote mode until the REN line is put in the local state, a Go To Local (GTL) command is received or the LCL front panel key is pressed.

DAV, NRFD, NDAC These are the "handshake" lines (Data Valid, Not Ready For Data and Not Data Accepted) which regulate the transmission of information over the lines DIO1-DIO8. For each command or data byte transferred, a complete handshake cycle occurs. This handshake is designed to hold up the bus until the slowest device has accepted the information. A description of the handshake cycle is given in the next paragraph, after the definition of the GPIB lines.

EOI When ATN is false, EOI (End Or Identify) indicates that the data on lines DIO1-DIO8 is the last byte of a data message. When the Wavetek 271 receives a data byte with EOI true, it automatically supplies a terminator character following the data byte. When the Wavetek 271 transmits the last byte of a message (which is always a terminator character) it also sets EOI true.

SRQ The Service Request line is used by the Wavetek 271 and other devices on the bus to signal the controller that they request attention. Since the SRQ line is common to all devices, additional tests must be made to determine which devices are signaling. The controller performs a Serial Poll to accomplish this.

IFC The Interface Clear line is asserted by the system controller to reset the interface logic in all devices connected to the bus to a known initial state.

3.6.3 Handshake Sequence

The three handshake lines, Data Valid (DAV), Not Ready for Data (NRFD) and Not Data Accepted (NDAC) are used in a typical data exchange as follows:

All devices currently designated as active listeners would indicate (via the NRFD line) when they are ready for data. A device not ready would pull this line low (ground), while a device that is ready would let the line float high. Since a low overrides a passive high, this line will stay low until all active listeners are ready for data. When the talker senses this, it places the next data byte on the data lines and then pulls DAV low. This tells the listeners that the information on the data lines is valid and that they may read it. Each listener (at its own speed) then takes the data and lets the NDAC line go high. Again, only when all listeners have let NDAC go high will the talker sense that all listeners have read the data. It can then remove DAV (let it go high) and start the entire sequence over again for the next byte of data.

3.6.4 GPIB Commands

Commands are sent over lines DIO1-DIO8 with ATN true they are divided into five classes:

1. Listen Addresses
2. Talk Addresses
3. Secondary Addresses
4. Universal Commands

   DCL Device Clear
   SPE Serial Poll Enable
   SPD Serial Poll Disable
   LLO Local Lockout

5. Addressed Commands

   GTL Go To Local
   SDC Selective Device Clear
   GET Group Execute Trigger

These commands and command groups are shown with their binary codes in Appendix A.

3.6.4.1 Listen Addresses

Listen addresses are used to command a device to read any data bytes transmitted over lines DIO1-DIO8. There are 31 different available addresses (hexadecimal codes 20 through 3E, ASCII codes SP through >). A 32nd address, called unlisten (hexadecimal 3F, ASCII ?) is used to command all devices to not read data bytes. The Wavetek 271 listen address is selected by internal switches (figure 2-2) or by front panel keyboard; e.g., ADRS 1 EXEC for address number one. Either method of selection specifies the lower 5 bits of the address (ref: table 2-2). Pressing the front panel ADRS key displays the GPIB address as a decimal device number. At power-on, the address is always that set by internal switches. Another internal switch (Figure 2-2) can lock out address selection by front panel keyboard if desired. Each time ADRS is pressed, XA will appear in the CMD RCL string. The address can not be reprogrammed from the GPIB.

3.6.4.2 Talk Addresses

Talk addresses are used to command a device to transmit data over lines DIO1-DIO8. There are 31 different available addresses (hexadecimal codes 40 through 5E, ASCII codes @ through ^). A 32nd address, called untalk (hexadecimal 5F, ASCII _) is used to command all devices to cease talking. The lower 5 bits of the Wavetek 271 talk address are selected by the same switches used to select the listen address. Thus, if the Wavetek 271 listen address is hexadecimal 21 (ASCII !), the talk address is hexadecimal 41 (ASCII A). Pressing the front panel ADRS key displays the GPIB address as a decimal device number.

NOTE: As shown in section 3.5 of the manual, use this decimal device number for programming both talk and listen commands. Separate talk and listen addresses are not used in program commands.

3.6.4.3 Secondary Addresses

Secondary address are used following a talk or listen address to provide the ability to address more than the 31 devices provided for by simple talk or listen addresses. Secondary addresses are ignored by the Wavetek 271.

3.6.4.4 Universal Commands

Universal commands are used to command a device to perform designated actions. Universal commands are recognized at all times. Universal commands performed by the Wavetek 271 are:

1. Device Clear (DCL) — Resets the Wavetek 271 to the initial power-on settings. DCL affects all devices on the bus.
2. Serial Poll Enable (SPE) — Causes the instrument to engage in a serial poll by responding with the serial poll status byte when addressed as a talker. Data line DIO7 will be on, if service is being requested on the SRQ line. When the status byte is read, it is reset to an ASCII blank, and the SRQ line is released (of course, it may still be held down by other devices). The status byte is also available by reading the Wavetek 271 talk message number 1. When this message is read, the status byte is reset and the SRQ released as for the serial poll.
3. Serial Poll Disable (SPD) — Discontinues serial poll. Returns instrument to normal talk modes.
4. Local Lockout (LLO) — Causes the Wavetek 271 to enter a state where the front panel LCL key is inoperative. In this state, the keyboard is disabled and the instrument will only accept parameter changes through the GPIB. To enable keyboard control, the GPIB controller must place the REN line in the local state.

3.6.4.5 Addressed Commands

Addressed commands are used to command a device to perform designated actions. Addressed commands are recognized only when the instrument is addressed

as a *listener*. Addressed commands performed by the Wavetek 271 are:

1. Go To Local (GTL) — Commands the Wavetek 271 to go to the local mode.
2. Selective Device Clear (SDC) — Resets the Wavetek 271 to initial power-on conditions. SDC affects only the selected unit.
3. Group Execute Trigger (GET) — Causes the actions specified by the GET mode (XG) code. If the Wavetek 271 microprocessor is idle (i.e., not processing a previously sent programming string), a GET command will be completed within 2.5 ms of receipt. Otherwise, it will not be done until current programming is processed.

3.6.5 Using the GPIB

This GPIB section of this manual has deliberately been placed after the REMOTE OPERATION section, because in actual practice the GPIB is much easier to use than its description would indicate. Some points to remember when programming a GPIB controller:

1. It is not necessary to use separate listen or talk addresses, or to worry about the ASCII or hexadecimal equivalent of the address. Simply program the decimal device number, which is same number previously programmed into the Wavetek 271 with the internal address switches or the front panel GPIB ADRS key.
2. When using the standard WRITE command, it is not necessary to program the state of the ATN line, etc. The controller performs these "handshake" functions automatically. (Some controllers have an alternate command, such as COMMAND @, that will allow the advanced programmer access to individual commands such as "attention" and "unlisten".)
3. The GPIB mnemonics (DCL, GET, etc.) are *not* necessarily the actual commands used by the controller. For example, on the controller used to write the sample programs in this manual, the command with the GPIB mnemonic GET translates to an actual controller command of TRG @.
4. Controller GPIB commands are not part of the standardized BASIC computer language, and the commands will vary from one make of controller to the next. Refer to the GPIB programming manual for your make of controller.

SECTION 4
CIRCUIT DESCRIPTION

4.1 GENERAL DESCRIPTION

The Wavetek 271 Pulse/Function Generator consists of four major sections (figure 4-1): the microprocessor control section located on the microprocessor/power supply board, the operator interface located on the display board, the function generator section located on the function generator board, and the pulse generator, burst counter and data registers located on the pulse board. Each of these major blocks is described briefly in this general description and then in more detail in following paragraphs.

4.1.1 Microprocessor Control

The microprocessor (figure 4-2) is the clearinghouse for all control operations. Through its software program in Read Only Memory (ROM), the microprocessor accepts commands from the front panel keyboard or the IEEE-488 General Purpose Interface Bus (GPIB), then sends operating parameters to the function generator circuits and auxiliary circuits, stores these parameters in Random Access Memory (RAM), and controls the front panel display.

The microprocessor section contains the analog interface circuitry which decodes and holds status information for the function generator board. A sample-and-hold circuit provides four analog voltages to control the function generator. Power supplies in this section power all the circuits of the instrument.

4.1.2 Operator Interface

The operator interface located on the display board (figure 4-2), includes the front panel keyboard, the

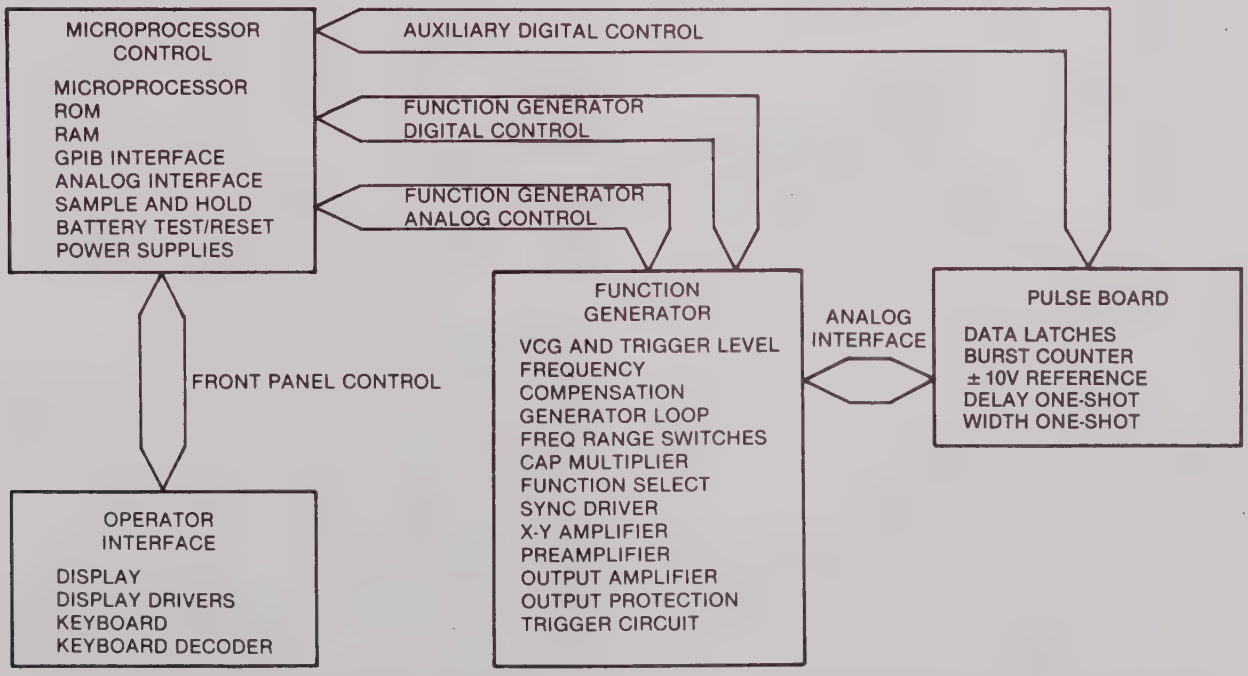


Figure 4-1. Major Blocks

fluorescent display, decoders and drivers. The microprocessor recognizes entries from the keyboard and performs the appropriate instruction. Display drivers transfer display information from the microprocessor to the 20 character, vacuum-fluorescent alpha-numeric display.

4.1.3 Function Generator

The basic generator loop, figure 4-2, contains a hysteresis switch which creates a triangle waveform by alternately switching equal positive and negative constant currents into a capacitor. The switching points are determined by comparing the triangle peak voltages against two reference levels. A complement of the switching waveform controls the trigger timing in the mode logic, drives the square shaper, and is buffered to provide the instrument's synchronization output (SYNC OUT). Decade values of capacitors determine the basic ranges for frequencies from 100 Hertz up. Below 100 Hertz, a capacitance multiplier scales down the triangle current to provide the four lowest decades of frequency in the instrument.

Within any selected frequency range, a Voltage Controlled Generator (VCG) circuit varies the triangle current proportionally to the frequency control voltage (FRQ) from the microprocessor section. This circuit also controls high frequency compensation by proportionately decreasing the reference levels to compensate for time delays.

The function select circuit chooses a buffered triangle wave, a square wave derived from the hysteresis switch, or a sine wave derived by a sine converter from the triangle wave. An X-Y multiplier circuit takes the current output from the function switch and, with its associated preamplifier, varies the waveform amplitude in proportion to the amplitude control voltage (AMP) from the microprocessor.

The output amplifier provides the final gain and output drive capabilities for the waveform, and sums offset from the amplifier into the signal as required. When the output signal peaks are programmed to be less than 1.0 volt, output voltage is attenuated by the decade output attenuator.

If excessive voltage is sensed on the output, the output protection circuit opens all the attenuator relays to protect the instrument. A voltage high enough to arc across the relays will blow a fast-acting fuse to further protect the instrument from major damage.

A trigger input circuit allows the generator to be triggered or gated externally. An internal control voltage (TRL) controlled by the microprocessor determines the level at which an external signal (at TRIG IN) triggers or gates the generator. The external trigger signal can also be gated directly into the square shaper to provide an external width function.

4.1.4 Pulse Board

The pulse board contains the pulse generator and burst counter circuits The pulse generator creates a pulse waveform of selectable delay and width. The burst counter enables the generator output for a predetermined number of output cycles when the burst mode is selected and the circuit is triggered. The pulse board also contains data registers to latch data from the buffered data bus to control other circuits on the board.

4.2 MICROPROCESSOR CONTROL CIRCUIT DESCRIPTION

The microprocessor control section and its associated circuits (figure 4-3) are located on the Microprocessor/Power Supply circuit board accessible beneath the bottom cover of the instrument. Descriptions in this section include the microprocessor/memory circuits, GPIB interface, battery test and reset circuitry, analog interface, sample and hold circuitry and instrument software.

The following descriptions refer to figure 4-3 and the microprocessor/power supply schematics in the back of this manual.

4.2.1 Microprocessor/Memory

The microprocessor/memory section includes the microprocessor itself, an address latch to demultiplex the lower order address bits, an address decoder to select appropriate memory locations or addressable registers, read only memory (ROM), random access memory (RAM), a data latch to hold data for transfer to analog and display registers, the beeper circuit, and the GPIB address switch and register.

4.2.1.1 Microprocessor

The 6803 microprocessor, U3, is in its expanded-multiplexed mode (mode 2), as determined by mode control programming diodes, CR1 and CR2. This mode allows the microprocessor to address external memory by using port 3 (P30-P37) as the multiplexed low-order address/data bus, port 4 (P40-P47) as the high-order address bus, with pins 39 and 38 as the address strobe and read/$\overline{\text{write}}$ line (R/$\overline{\text{W}}$) respectively. Ports 1 (P10-P17) and 2 (P20-P24) are always I/O ports.

A clock-generating circuit within the microprocessor uses an external 4 MHz crystal, Y1, between the XTAL 1 and XTAL 2 pins to develop its internal phase clocks and the 1 MHz system enable clock (E). Figure 4-4 shows

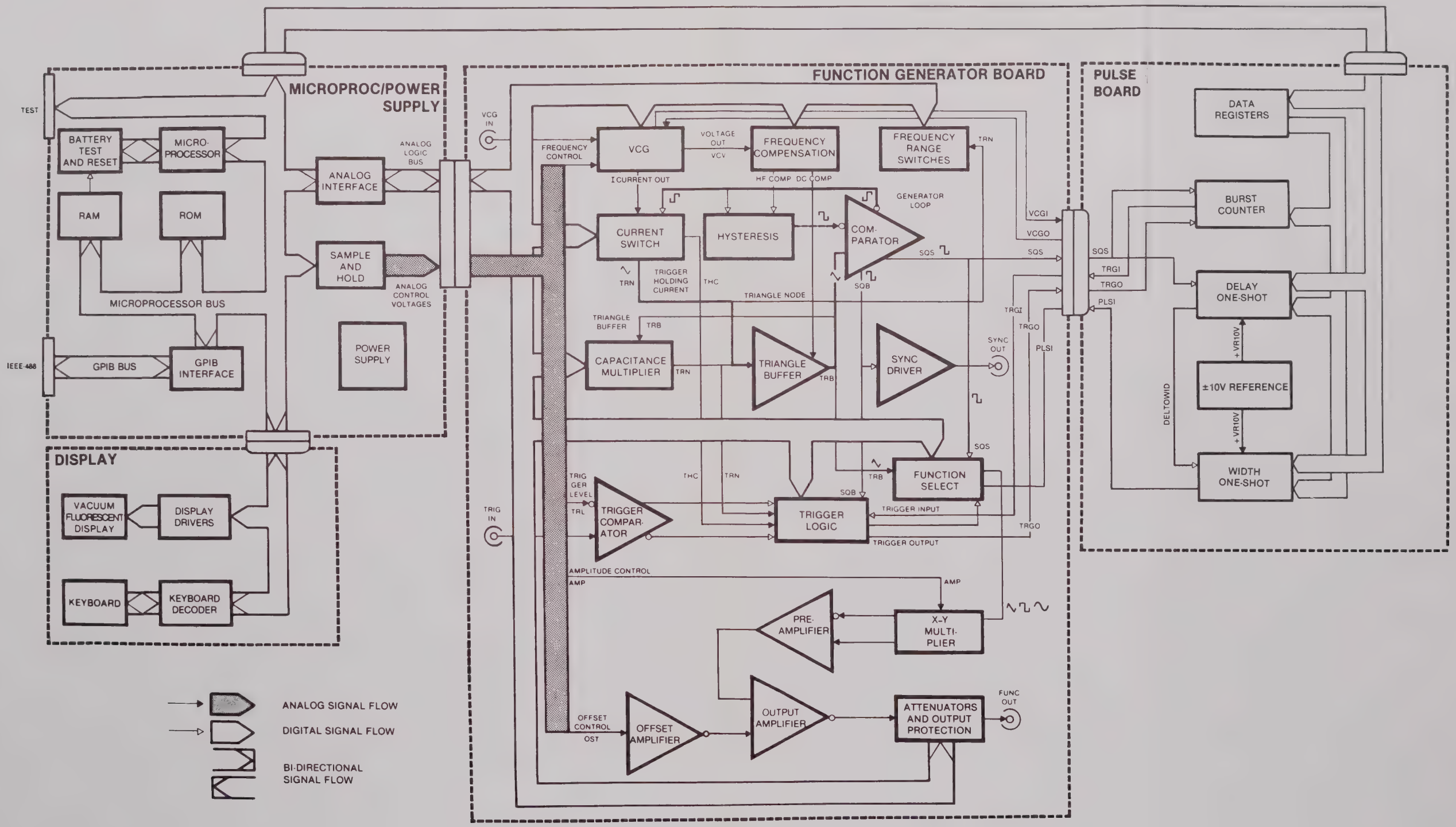


Figure 4-2. Functional Block Diagram

MICROPROCESSOR/MEMORY

GPIB INTERFACE

E
AS
R/W
NMI
BATV
BEEPER U2, Q1
BATTERY TEST U27
RESET CR1, CR2
P17
P22
P15
P14
IRQ
NMI
MR
P20
P22
PORT 2
MICRO-PROCESSOR
R/W
AS
ADR0-ADR7
ADR8-ADR15
PORT 1 P10-P17
P14
P15
P17
P2
TEST
E
R/W
WRITE PULSE U1
WRP
ADDRESS LATCH U4
AD0-AD7
ADR0-ADR7
ROM1
ROM2
ROM U9, U10
ADR0-ADR12
AD0-AD7
RAM1
RAM2
RAM U11, U12
WRP
BATV
ADR0-ADR10
AD0-AD7
IRQ
E
R/W
MR
GPIB
ASE
GPIB INTERFACE U6
T/R
T/R2
ADR0-ADR2
AD0-AD7
GPIB BUS DRIVERS U7, U8
J2
ADR8-ADR15
ADDRESS BUS, ADR0-ADR15
AD0-AD7
TEST
ADDRESS/DATA BUS, AD0-AD7
GPIB ADDRESS U5, SW1
ADR0
ADR0,ADR1,ADR3,ADR4
TEST
E
GPIB
RAM2
ROM1
ROM2
RAM1
ANALOG
TESTSEL
ADDRESS DECODER U13
ADR2-ADR15
DISP
KYBD
ADR0-AD7
DATA LATCH U25
ANALOG INTERFACE
ANALOG DECODER U14
AR0-AR3
ANALOG REGISTERS
ANL0-ANL27
J6 ANALO
ANA0
ANA2
ANA3
DISPLAY
ANOA-ANOO & ANODP
VACUUM FLUORES-CENT DISPLAY V1
SEGMENT AND DIGIT DRIVERS U1, U2, U3, U4
GRID 1-20
FILAMENT DRIVER U8
ADR0
ADR1
DATA0-DATA7
LATCHED DATA BUS, DATA0-DATA7
DATA0-DATA7
ADRB-ADR3
AD0-AD4
P7
J7
AD0-AD4
DISP
DSP
BLANK
KYBD
DISP
P16
P21
KYBD
PORT 1, P10-P17
KEYBOARD
KEYBOARD DECODER U6, U7
P10
P11
P12
P13
P12
P13
AUX BUF-FERS
J4 AUX
ANA0
ADR0
DAC U15, U16
SAMPLE AND HOLD
SH0
SH1
SH2
SH3
SAMPLE AND HOLD

ANALOG SIGNAL FLOW

DIGITAL SIGNAL FLOW

BI-DIRECTIONAL SIGNAL FLOW

Figure 4-3. Microprocessor Control and Display Block Diagram

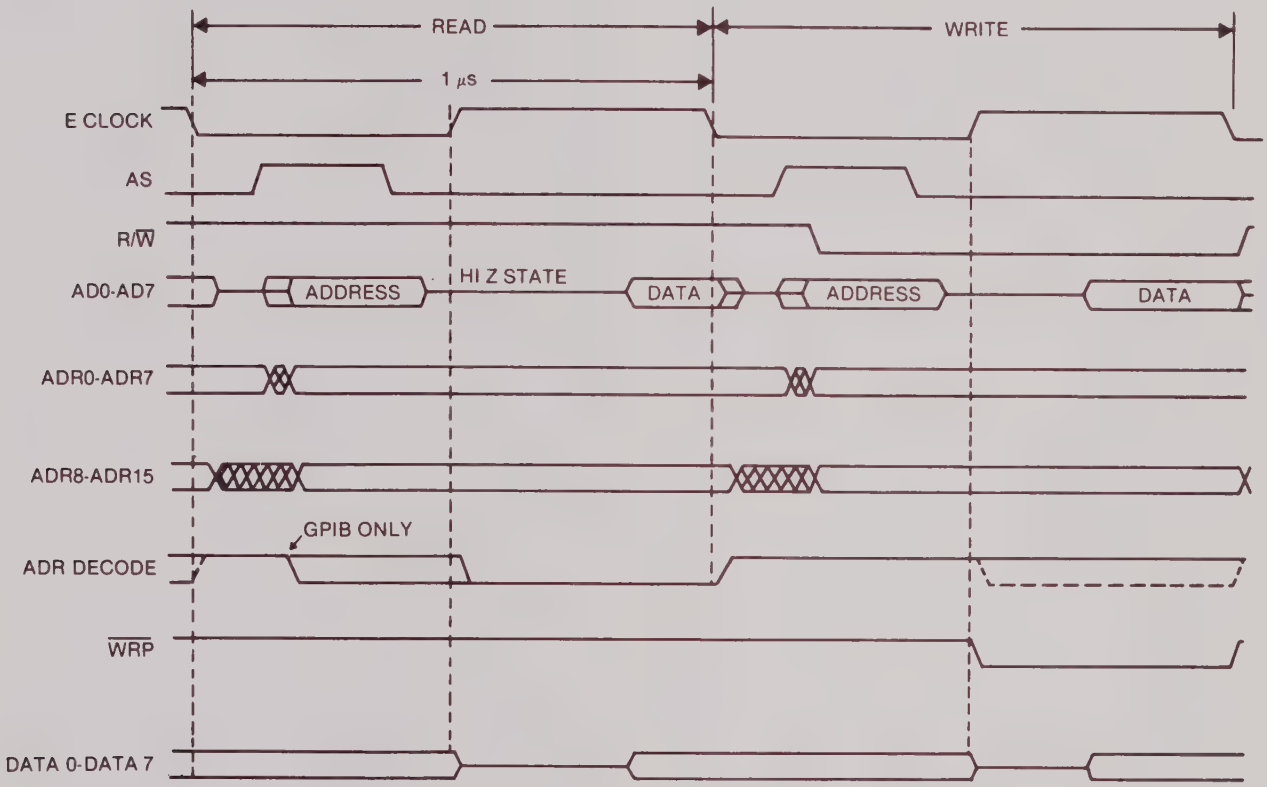


Figure 4-4. Microprocessor Timing Diagram

the approximate timing for major signals and busses in the microprocessor/memory system. Actual system timing varies somewhat from instrument to instrument, so signal spacing may be different within the 1 μs period of the system clock.

The microprocessor responds to three interrupt inputs: master reset ($\overline{\text{RESET}}$), which initializes the microprocessor; the external interrupt request line ($\overline{\text{IRQ}}$),which the GPIB interface uses to signal the processor; and the non-maskable interrupt ($\overline{\text{NMI}}$), which is not used in the instrument, but is available on the test connector.

4.2.1.2 Address Latch

An octal latch, U4, demultiplexes the address/data bus from the microprocessor to hold the low-order addresses (ADR0-ADR7) during the part of the E clock cycle that data occurs on the multiplexed bus. Latching occurs on the negative transition of the AS signal (U3, pin 39). See timing diagram, figure 4-4.

4.2.1.3 Data Latch

Octal latch, U25, demultiplexes data from the address/data bus much the same way as the address latch (U4), except that the falling edge of the E clock, rather than AS, is used to latch the data.

4.2.1.4 Address Decoder

A field programmable gate array, U13, decodes the upper 14 bits of the 16 address lines to select one of eight possible addressable devices or circuits. These are the keyboard decoder ($\overline{\text{KYBD}}$), display drivers ($\overline{\text{DISP}}$), IEEE-488 interface ($\overline{\text{GPIB}}$), RAM location 1 ($\overline{\text{RAM1}}$), RAM location 2 ($\overline{\text{RAM2}}$), ROM location 1 ($\overline{\text{ROM1}}$), ROM location 2 ($\overline{\text{ROM2}}$), and the analog interface registers ($\overline{\text{ANALOG}}$). In addition, a ninth output decodes the reset and interrupt vector addresses into ROM2 for normal operation, but allows a test input to direct these vectors into external memory. A memory map, table 4-1, shows the position in memory for each of the above blocks.

4.2.1.5 ROM

Two read-only-memories, U9 (ROM1) and U10 (ROM2), contain the program for the microprocessor. Their respective locations in memory are adjacent as shown in the memory map, table 4-1. $\overline{ROM1}$ and $\overline{ROM2}$ from the address decoder enable the appropriate IC on the rising edge of E clock. A brief description of microprocessor operation will be covered in the software section.

Table 4-1. Memory Map

Addressable Devices	Address (Hexadecimal)
Internal Register	$0000—$001F
Analog	$0020—$003F
DISP, GPIB (See Note 1)	$0040—$005F
KYBD & Not Used (See Note 2)	$0060—$007F
Internal RAM	$0080—$009F
≈ Not Used	$0100—$9FFF ≈
ROM 1	$A000—$BFFF
ROM 2	$C000—$DFFF
RAM 1	$E000—1E7FF
RAM 2	$E800—$EFFF
≈ Not Used	$F000—$FFEF ≈
Vector (ROM 2) (See Note 3)	$FFF0—$FFFF

Notes

1. DISP $40—143, GPIB $58—$5F
2. KYBD $60—$6F, Not Used $70—$7F
3. Alternate addresses for last 16 locations in ROM 2.

4.2.1.6 RAM

The microprocessor uses two random access memories, U11 and U12, as a scratch pad memory and as memory for stored settings. The $\overline{RAM1}$ or $\overline{RAM2}$ line from the address decoder enables the selected RAM on the rising edge of the E clock. During a write cycle, the write pulse circuit ANDs the read/$\overline{write}$ line from the processor (R/$\overline{W}$) with the E clock to generate a write pulse ($\overline{WRP}$) after all address lines have become stable. A lithium battery (BT1) maintains a sufficient voltage level to prevent the loss of information stored in both RAMs when external power is removed. Schottky diode CR5 conducts when the + 5V supply falls below the battery's voltage (approximately 3V). Diode CR4 prevents the battery from discharging through the rest of the circuit.

4.2.1.7 Beeper

The microprocessor generates a 62.5 kHz signal continuously at port 22 (P22) after start-up procedure is complete. To generate an audible beep, the processor sends a positive pulse from port 17 (P17) to the reset line of a 12-bit ripple counter, U2. The counter reset condition enables the 62.5 kHz signal from port 22 to the clock input of the counter. The fifth stage output of the counter drives a transistor switch which in turn drives the beeper at approximately 2 kHz. When the eleventh and twelfth states of the counter both go positive, U1-3 inhibits the 62.5 kHz signal from the processor and stops the beeper. This gives a beep about 50 ms long.

4.2.1.8 GPIB Address

An 8 section DIP switch (SW1), selects the GPIB address for the instrument. Since IEEE-488 specifications allow only 31 possible addresses for GPIB instruments (binary 0-30), only the first five switches S1-S5 (GA0-GA4), are used to select the actual address. S6 (FPADEN) enables or disables the front panel address entry capability. A momentary closure of S7 resets the elapsed operating time counter in the microprocessor. S8 is not used.

An inverting tri-state buffer, U5, gates the address switch information onto the multiplexed address/data bus when enabled by the address switch enable line (ASE) from the IEEE-488 interface device.

4.2.2 GPIB Interface

The GPIB Interface section of the microprocessor board interfaces with the instrument's microprocessor and handles all the handshake protocol and data transfer over the IEEE-488 General Purpose Interface Bus (GPIB).

Most of the IEEE-488 instrument bus protocol functions are handled by the General Purpose Interface Adapter (GPIA), a single IC, U6. Data and control portions of the bus require high current driving capability and specific line termination which the Bus Drivers, U7 and U8, provide. These two sections of the bus have different requirements depending on whether the instrument is acting as a talker or a listener: the data transceiver, U7A or U7B, always acts as a transmitter during talk modes and a receiver during listen modes, but the control transceiver requires that some lines transmit while others receive in both of these modes. These different requirements are met in the "A" transceivers by using different parts for each function (the 75160A for data and the 75161A for control) or in the "B" transceivers by using an extra control line (pin 11 on the 3447.) The instrument is able to use either type of bus transceiver scheme.

The IEEE-488 Interface IC, U6, does all the handshaking requirements of the 1978 IEEE-488 standard. When the controller on the bus sends either the instrument's talk or listen address or a serial poll, U6 signals the instrument's microprocessor by asserting the interrupt request line, $\overline{IRQ}$ (a low on U6, pin 40). The processor can then interrogate any of the eight registers internal to U6. Data from the IEEE-488 bus (listen mode) is accessed by reading from the data registers in U6; data output (talk mode) is written to the same register. The address strobe enable line ($\overline{ASE}$) from the interface IC, U6, controls the select line to U5 that enables the GPIB address switch, SW1. The microprocessor can read this switch by a read of the address register in U6, which causes U6 to set $\overline{ASE}$ low during the E-clock (data) portion of the microprocessor clock cycle. This address is not necessarily the address used by the interface IC (U6); that address is stored in U6 by writing into the internal address register. The actual address of the instrument can be changed by front panel control, but will return to the address specified by the GPIB address switch during a microprocessor reset cycle (power-up).

During the microprocessor reset cycle (power up), $\overline{MR}$ to U6 pin 19 ($\overline{RESET}$) inhibits all the outputs to the bus drivers and the drivers themselves to prevent false information from being transmitted over the bus. In addition, to prevent a false service request message state (SRQ asserted), port 20 from the microprocessor scans the SRQ line at U6, pin 23 to keep a program monitor of the status of the SRQ flag out of U6. A false state could otherwise occur if a very fast controller addressed the instrument in quick succession before the instrument's microprocessor had time to reset SRQ.

For a complete definition of the GPIB lines, refer to paragraph 3.6 in the OPERATION section of the manual.

4.2.3 Battery Test and Reset

One-half of dual operational amplifier U27 acts as a voltage comparator to detect low voltage on the battery, BT1. When the microprocessor goes through its power up procedure and every six minutes thereafter, the processor strobes port 15 (P15) to a low state to simulate the battery's normal load when power is shut off, then checks the output of the comparator at port 14 (P14). If the battery voltage drops below +2.4V, the comparator goes high and the processor sets an internal flag. At power up, this flag causes an immediate display warning for low battery; after power up, a reset command, storing a stored setting or recalling a stored setting causes the warning display or an SRQ, depending on whether the command originates from the keyboard or the GPIB bus.

The second half of U27, acting as a comparator, serves as a microprocessor reset circuit. During power up, diode CR19 is reverse biased, allowing the positive input to U27 (pin 5) to rise to the voltage determined by R59 and R60 (approximately +4.7V). With CR18 forward biased, the negative input to the comparator (U27, pin 6) rises more slowly, at the time constant determined by R57 and C72 (about 100 ms). Since it takes about two time constants for the negative input to charge as high as the positive input, about 200 ms elapse before transistor Q2 is turned off and the $\overline{RESET}$ line to the microprocessor is allowed to rise. When power to the instrument is shut off and the +5V line begins to drop, diode CR18 is reverse biased and the negative input to the comparator falls at the same rate as the +5V line. Diode CR19 is forward biased, so the voltage at the positive input falls more slowly. When the +5V line falls slightly below +4.75V, the comparator turns on Q2 and keeps the microprocessor reset as the power continues to fall.

4.2.4 Analog Interface

The analog interface consists of an analog decoder that decodes addresses in the analog section of memory, analog registers that hold digital information for the function generator board, and auxiliary buffers that route data to the pulse board.

4.2.4.1 Analog Decoder

When the microprocessor selects the analog section of memory ($\overline{ANALOG}$ goes low), a 2 to 4 line decoder (U14A) decodes the 32 bytes of memory from ADR3 and ADR4 into four, 8-byte blocks ($\overline{ANA0}$-$\overline{ANA3}$). $\overline{ANA0}$ selects the digital-to-analog converter, U15. $\overline{ANA1}$ is decoded further from ADR0 and ADR1 by U14B to select the analog registers ($\overline{AR0}$-$\overline{AR3}$). $\overline{ANA2}$ and $\overline{ANA3}$ select registers (including registers internal to the DACs) on the pulse board.

4.2.4.2 Analog Registers

The analog registers hold the analog control logic for the function generator board, ANL0-ANL27, and the four sample-and-hold select lines. Latched data (DATA0-DATA7) is strobed into registers U21 through U24 by the falling edge of the analog register control lines, $\overline{AR0}$ through $\overline{AR3}$ respectively. ANL0 through ANL27 appear at the analog connector, J6.

4.2.4.3 Auxiliary Buffers

The tri-state auxiliary buffers, U28 and U29, prevent the latched data lines from injecting noise through the auxiliary connector (J4) to the pulse board by inhibiting the buffers except when the pulse board registers are being addressed. One-half of U28 (input pins 2,4,6,8) is continuously enabled, but the signals at its inputs do not change until the microprocessor selects the auxiliary registers. At this time, the buffered port 12 (P12) enables the buffered data (BDATA0-BDATA7) and buffered address (BADR0- BADR2) lines.

4.2.5 Sample and Hold

The sample-and-hold section consists of the DAC (digital-to-analog converter), U15, the −10.24V reference for the DAC, and four sample-and-hold circuits that demultiplex the DAC output to provide four separate analog control voltages for the function generator board.

4.2.5.1 DAC

The 10-bit digital-to-analog converter, U15, contains its own internal registers for latching data and interfaces directly to the latched data bus (DATA0-DATA7). When the microprocessor transfers data into the DAC with ADR0 high (approximately every millisecond), the negative transition of $\overline{ANA0}$ latches the most significant 8 bits from the data lines into the DAC's internal register. A second transition of $\overline{ANA0}$ with ADR0 low latches the least significant bits. The current output of the DAC (U15 pin 12) is converted to a voltage output by operational amplifier U16A at pin 1 using a feedback internal to the DAC at U15 pin 14.

4.2.5.2 −10.24V Reference

Since the DAC circuit provides an inverted programmable portion of the reference voltage, the reference must be negative to get a positive output. This adjustable negative voltage is generated by operational amplifier U16B in an inverting configuration with a gain of less than −1 and using the highly regulated +15V power supply as its input. R16 adjusts the voltage for precisely −10.24V corresponding to a 10 mV step for each binary step of the DAC.

4.2.5.3 Sample and Hold

The microprocessor sequences the DAC through four discrete voltages at about 1 ms each (4 ms for a complete cycle). The four sample-and-hold circuits latch each of these analog voltages in turn to provide the four separate analog control voltages to the function generator board, SH0 through SH3, appearing at J6. In the following paragraph, component designations refer to the first sample and hold section that generates SH0 (corresponding to frequency control, FRQ, on the function generator board). The other sample and hold circuits act similarly.

Within a few microseconds after the appropriate voltage appears at the output of the DAC circuit, the sample-and-hold control line from U24 pin 12 turns on the analog switch U17A and the DAC output charges the holding capacitor C28. Since the analog switch, U17A, transmits a small charge from its logic input (pin 1) to the analog output (pin 3), an inverter, U18F, generates an opposing signal and the capacitor, C27, injects the opposite charge to cancel the effect. Because these charges do not exactly coincide in time, the result is a high-frequency bipolar spike that must be eliminated. A two-stage filter consisting of R18, C29, R19 and C30 accomplishes this. The holding capacitor C28 continues to charge until the next sequence is due. The control signal from U24 pin 12 turns analog switch U17A off before loading the following circuit's DAC information at U17D. The analog switch's high output impedance in the "off" state and the high input impedance of the buffer at U19B maintain the voltage on the output of the circuit with negligible discharge until the next cycle selects this sample-and-hold circuit again.

4.2.6 Power Supply

Four power supply voltages, +15V, −15V, +5V and +45V (figure 4-5) are generated on the microprocessor/power supply circuit board. The pass elements for each of the supplies are three-terminal regulators (VR1, VR2, VR3 and VR4) which normally operate with a 1.25V difference between their output and reference terminals. The +5V and +45V supplies use very little additional circuitry. In these simpler supplies, the reference voltages are provided by a resistor divider.

4.2.6.1 +5V Supply

In the +5V supply (Microprocessor/Power Supply Schematic, sheet 3), ac from the transformer, T1 (located on the rear panel), is rectified by CR13 and filtered by C56 and C57 to provide unregulated dc for the regulator, VR3. Resistive divider R49 and R50 sets the voltage at the reference input, pin 3, to provide an output of +5V

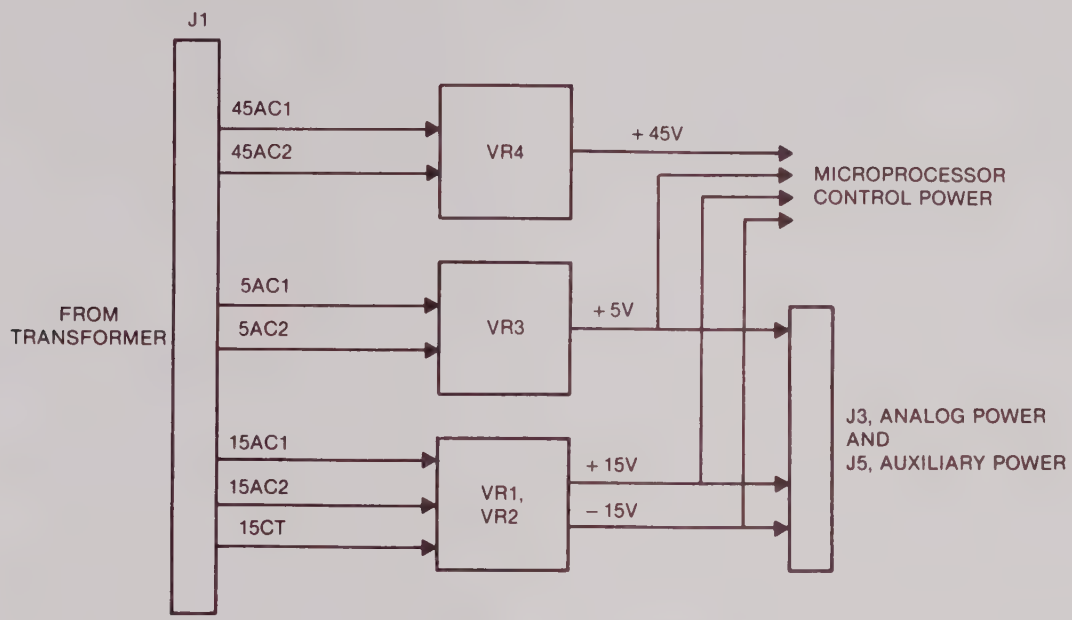


Figure 4-5. Power Supply

± 5% at E2, while C58 and C59 provide additional filtering at the output of the regulator. R53 loads the supply to guarantee operation of the regulator if the + 5V test jumper is removed. CR14 prevents C59 from discharging back through the regulator when power to the instrument is turned off.

4.2.6.2 + 45V Supply

The + 45V supply operates much the same as the + 5V supply except that the unregulated dc at VR4 pin 1 and the regulated output voltage (at pin 2) are much higher. The divider, R52 and R51, sets the output slightly below + 45V so the 5% tolerance of the regulator cannot give an output greater than + 45V.

4.2.6.3 ± 15V Supplies

The + and – 15V supplies that power the analog sections of the instrument require greater accuracy and stability than the basic regulator provides, so some additional circuitry is necessary. In the + 15V supply, the operational amplifier, one-half of U26, compares a portion of the output voltage with a stable zener reference diode, CR10. The op-amp's inverted output drives the reference input of the regulator to compensate for any error in the output. Since the op-amp output cannot operate within 1.25V of its positive supply voltage, a divider, consisting of R35 and R36, allows the output to operate near ground potential. R33, which is in series with the output of the regulator, causes current regulation to take place at a lower value than the internal limiting that the regulator provides. As the current through R33 reaches its limiting value, the voltage drop across R33 reaches 1.25V, the normal voltage difference between the regulator output and reference pins. Any further current through R33 now creates a greater than 1.25V drop that the regulator senses at VR1 pin 3 as an overvoltage and responds by decreasing its output voltage until the current falls back to the limiting value. Diode CR9, in series with the op-amp output (U26 pin 1) prevents the op-amp from sourcing any extra current through R35 that would change the output current limit. A small current through R34 keeps the op-amp in its operating range up to the current limit. C69 and C70 speed up the external regulation to match the internal regulator. R39 allows the output to be adjusted to precisely + 15V.

The – 15V supply operates similarly to the + 15V supply, but the polarities are reversed and the op-amp tracks the + 15V supply rather than using another zener as a reference. R47 adjusts the – 15V supply.

4.2.7 Microprocessor Software

Although a detailed description of software is beyond the scope of this manual, some discussion of the microprocessor operation is helpful in understanding how the instrument functions.

Figure 4-6 shows the three main program loops for microprocessor operation: a fast background loop, a slow background loop, and the parser-procedure loop. The background loops only check registers for interrupt flags set by external or timer interrupts. The parser selects and calls procedures when the program enters it, and returns control to the fast background loop when a procedure is finished.

4.2.7.1 Fast Background

The fast background loop inspects the three internal registers (GPIB, keyboard and timer) for interrupt flags (non-zero states) and then returns to its beginning. If no interrupt flags are set, the entire loop takes only about 50 to 60 μs. If a flag is set, the loop time increases by the length of the interrupt procedure. If either of the first two register flags (GPIB or keyboard) are set, the background program calls the parser. When the parser completes an operation, it returns the program to the beginning of the fast background loop. If the timer register flag is set, the program enters the slow background loop.

4.2.7.2 Slow Background

The timer flag in the fast background loop looks for an overflow in the 2^{16} bit (which occurs about every 66 ms)

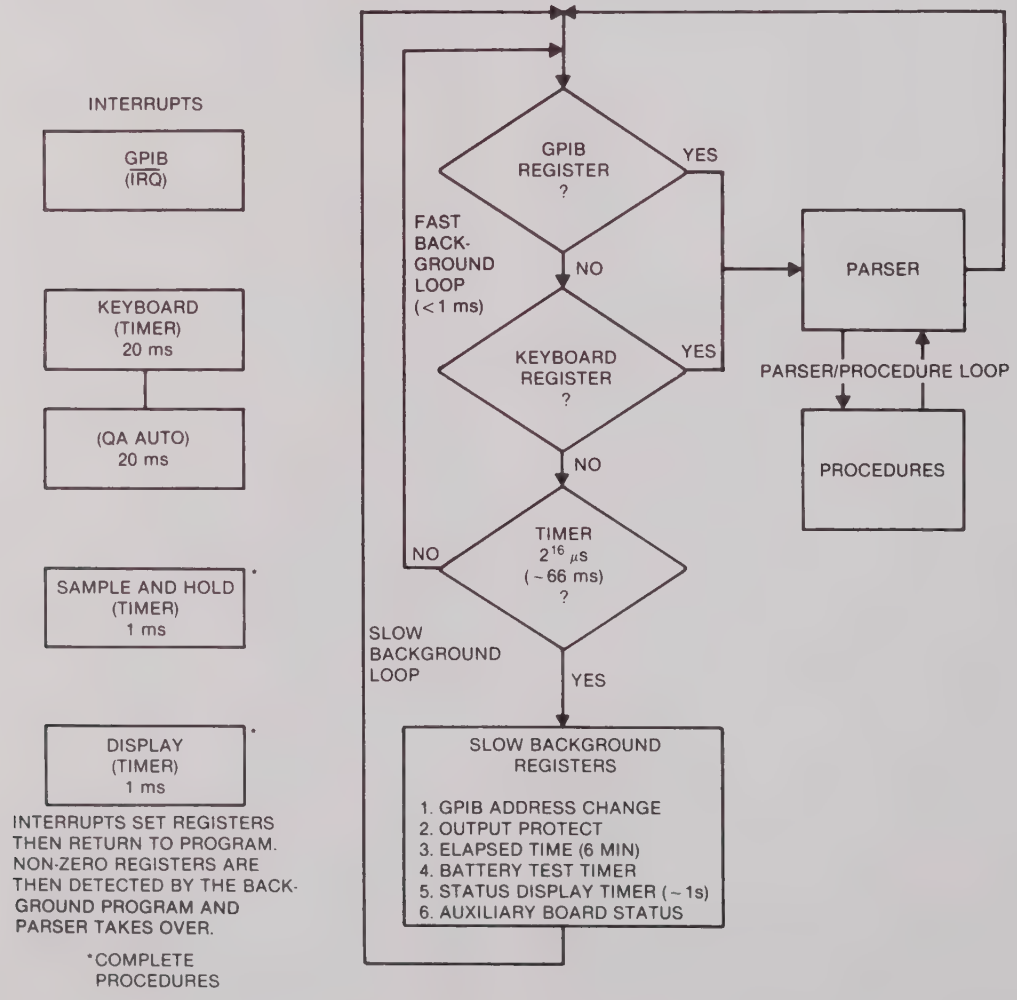


Figure 4-6. Program Loops

of the timer counter (part of the microprocessor IC). The slow background loop then examines a series of other registers: GPIB address change, output protection flag, elapsed time (with its associated battery test timer), a status display timer, and an auxiliary board status flag.

Address Change. The GPIB address change actually compares two sets of two registers: it compares the stored keyboard-entry address, (if enabled) with the register in the GPIB interface and if they are different, enters the new value in the interface; it also compares the previously stored value of the internal address switch with the current setting of the switch, and if they are different, enters the new switch setting in the switch storage location, the GPIB interface, and the front panel register. In addition, if the keyboard entry is disabled, it inhibits the first comparison. The elapsed time counter is reset at this time if the reset section of the switch, SW1 (ETR) changes.

Output Protection Flag. The output protection flag initiates a short routine, when set, that displays the front panel output protection error message, sets SRQ in the GPIB interface, initiates an extended warning beep by repeating 32 beep activations spaced by a timer, and opens up all the output relays on the function generator board.

Elapsed Time Flag. The elapsed time flag is set at 6 minute intervals by the timer. It updates the elapsed time counter (adds 0.1 hr) and initiates the battery test timer. The battery test routine loads the battery for about 120 ms then checks the battery test circuit for low battery voltage. If the battery is low, the routine sets a flag that causes a store, recall, or reset command to display a low battery warning, give a double beep and set SRQ.

Status Display Timer. The status display timer works only when the instrument is set to display status. At intervals of about 1.17s, the timer flag is set and the next background pass causes the equivalent of a cursor command to the instrument, advancing the status display.

Auxiliary Board Status. The auxiliary board status lines is not used in the Wavetek 271.

4.2.7.3 Parser/Procedure

The parser handles all programming chores except short housekeeping routines. When the parser is called, it examines a series of registers and decides which routines are required, then calls the required procedure which, when complete, returns control to the parser. When the parser has scanned all the condition registers, it returns control to the fast background. Even if their functions appear simple, the parser and the procedures with their interpretive functions make up the bulk of the program.

4.2.7.4 Interrupts

There are only two ways the processor program can be interrupted: through $\overline{IRQ}$ (generated by the GPIB interface) or through an internal timer (used for all other interrupt requirements).

GPIB Interrupts. GPIB interrupts are initiated by the GPIB responding to GPIB bus commands. When the interrupt occurs, a byte is read from the GPIB interface and stored in a register. The program then returns to its pre-interrupt position. It is the fast background program that actually inspects the register and passes control to the parser, which in turn decides what routines are called to process the information.

Timer Interrupts. Certain subroutines are run during initial power-up and periodically during the time the instrument is on. These subroutines are initiated when the number in the clock register (within the microprocessor) matches the preset number in any of the interrupt registers (within the microprocessor). Upon completion of the subroutine, the preset number corresponding to the elapsed time required between successive interrupts for the function is again added to that interrupt register. The clock timer continues to increment its own register, and when the number in this register again matches the interrupt register, the subroutine is initiated. These interrupt registers work independently of each other and may set another register (as in the keyboard interrupt) or they may initiate an entire subroutine.

4.3 OPERATOR INTERFACE CIRCUIT DESCRIPTION

The operator interface section is located on the display circuit board, which is mounted behind the front panel. Included are the display circuits (consisting of the segment drivers, digit drivers, the filament driver, and the display), and the keyboard circuits (consisting of the keyboard decoder and the keyboard).

Refer to the display schematic in the back of this manual for circuits described in the following paragraphs.

4.3.1 Display

The display circuit consists of vacuum fluorescent display, V1, filament driver, U8, segment drivers, U1 and U2, and digit drivers, U3 and U4. The display is strobed on, one digit at a time, by the microprocessor.

The microprocessor controls the display multiplexing. A 1 ms timer interrupt initiates a display scan routine that advances one digit at a time on the display and enters the appropriate decoded drive information. After the twentieth digit (20 ms), the microprocessor resets an internal counter, and the digit scan repeats.

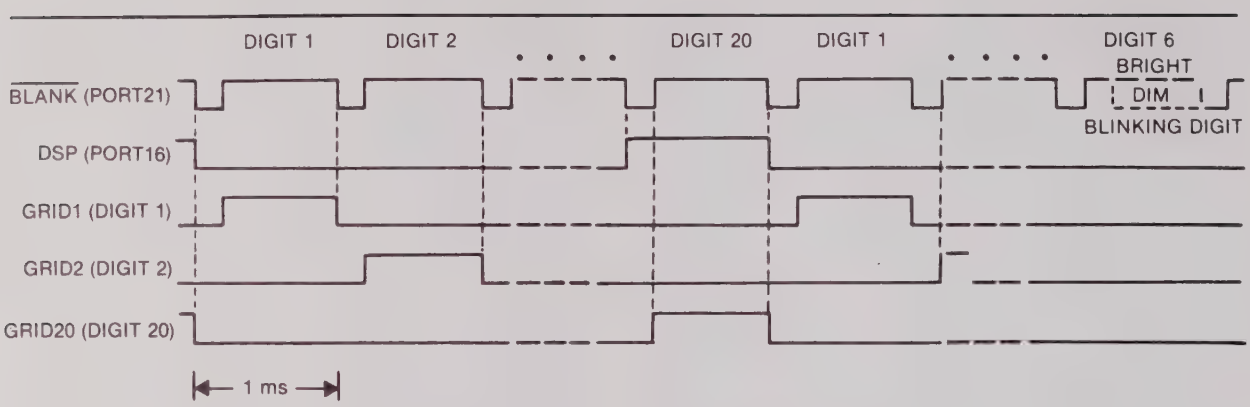


Figure 4-7. Display Digit Timing

Figure 4-7 shows the digit timing sequence for the display. The interrupt timer in the processor sets $\overline{\text{BLANK}}$ (Port 21) low. Inverted by U5E, this signal disables all display drivers (which blanks the display) and advances the shift register in the digit drivers, U3 and U4. After about 200 μs, $\overline{\text{BLANK}}$ returns to its high state and the appropriate digit is enabled (GRID1-GRID20). When the processor's scan counter reaches 20, it sets the digit scan position line.

During the time $\overline{\text{BLANK}}$ is low, the processor recalls the digit information already decoded for the 16 segment display and stores this data in latches within segment drivers U1 and U2. The display segment timing is shown in figure 4-8. About 120 μs after the falling edge of the $\overline{\text{BLANK}}$, the processor loads the two-byte segment data into the segment driver registers. $\overline{\text{DISP}}$ from the address decoder strobes the buffered data (DATA0-DATA7) into U1 (lower order byte) or U2 (upper order byte) determined by ADR0 and ADR1. The rising edge of $\overline{\text{BLANK}}$ then enables the output lines (ANOA-ANOO and ANODP) to drive the segment anodes of the display.

In the vacuum fluorescent display, all segment lines are common and individual grids enable each digit. Display filament power is provided by the driver circuit which is an IC timer, U8, configured as a 50 kHz oscillator with a 40% duty cycle. Since the output at U8 pin 3 swings from 0 to + 15V, the average dc level is about + 6V. This allows the grid lines to pull 6V negative with respect to the filament, which also serves as the cathode. Capacitor C14 acts as an ac ground to maintain a constant dc level across the entire length of the filament.

4.3.2 Keyboard

The keyboard section of the operator interface consists of the keyboard itself, (a 45 switch array mounted just

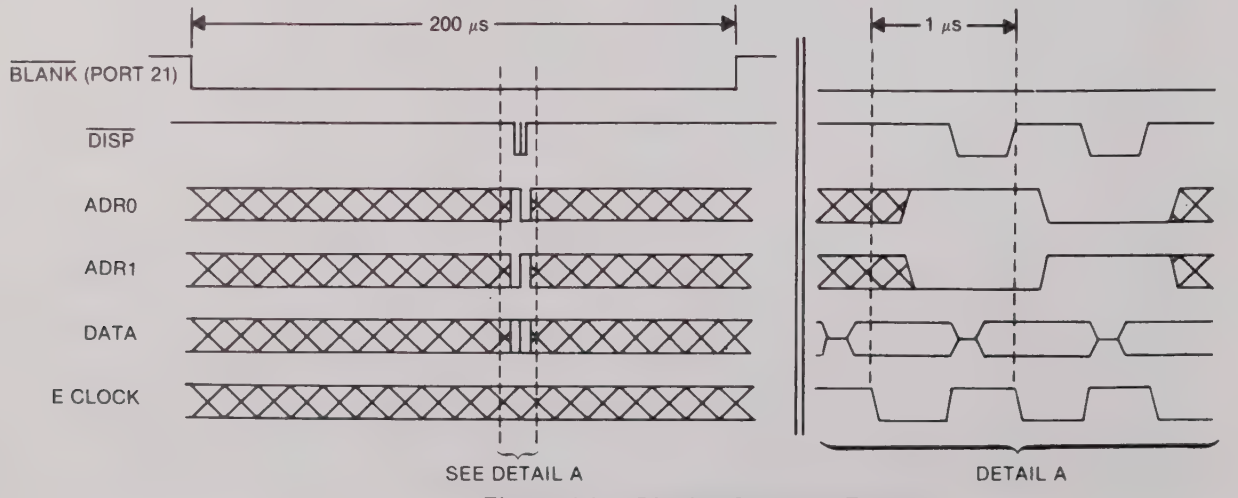


Figure 4-8. Display Segment Timing

behind the front panel overlay), and the keyboard decoder, U6 and U7, mounted on the display board.

The keyboard is an X-Y matrix of switches. Scanning pulses are applied to the columns of the matrix by U7, and key closures are detected at the matrix rows by U6.

Every 20 ms, the processor scans the keyboard decoder as a series of memory locations. A 4-to-10 line decoder, U7, decodes the four low-order latched address bits (ADR0-ADR3) to the 9-line side of the 9 by 5 switch array. If the operator presses a key on the front panel, the closed contact allows the appropriate decoded address line from the inverting output of the 4-to-10 line decoder (U7) to pull down 1 of 5 pull-up resistors in R3. During the data valid part of the E-clock cycle of the processor, $\overline{\text{KYBD}}$ from the address decoder enables the tri-state buffer, U6, and the processor reads a low at 1 of 5 bits on the address/data bus. The processor can then call the appropriate routine for the key pressed. If the keyboard scan finds no key pressed, the processor returns to its normal routines.

4.4 FUNCTION GENERATOR CIRCUIT DESCRIPTION

The function generator circuit board is accessible beneath the top cover of the instrument below the swing-up pulse board. This section includes the VCG and trigger level circuits, the basic generator loop, frequency range switches, capacitance multiplier, frequency compensation circuits, sync output driver, trigger circuit with mode logic, function select circuit including the sine converter and square logic, X-Y multiplier, preamplifier, offset amplifier, output amplifier and output protection circuits.

Refer to the function generator schematic in the back of this manual for circuits described in the following paragraphs.

4.4.1 VCG and Trigger Level

The VCG circuit converts a 0 to + 10V control voltage from either the microprocessor board or the external VCG input to positive and negative currents that control the frequency of the generator loop. The input stage acts as a summing amplifier. The control voltage from the processor board, FRQ (normally between + 1 and + 10V), develops a current through R4 and R5 into the summing node, pin 2 of U2A. R4 and R5, with C1, also act as a filter for the FRQ line to reduce the microprocessor switching noise. The first stage has a gain of approximately − 0.4, so its output at U2A pin 1 ranges typically 0.4V to − 4.0V. When the external VCG input is used, FRQ is normally set to 0V by programming FREQ 0, EXEC from the front panel, and the voltage from the external VCG input across R6 now determines the first stage output. CR1 and CR2 prevent excessive voltage at VCG IN from damaging the VCG amplifier. For frequencies between 10 MHz and 12 MHz, an overrange control, $\overline{\text{OVR}}$, adds a fixed 0.2 mA through R1 and R2 to increase the maximum voltage out of the first stage (or current out of the entire VCG circuit). The 10 kHz to 99.9 kHz range control, $\overline{\text{FR5}}$, increases the current from FRQ by paralleling R3 across the series combination of R4 and R5. This increase compensates for the larger relative capacitance on this range due to the minimum triangle node capacitance (C43 and C44) added to the smallest fixed range capacitor (C50). A gain adjustment (R8) in the first stage is used to control the top-of-range frequency. R11 controls the first stage offset to zero the low end of the external VCG input.

With the VCG jumper in its normal operating position (E9 to E10), the first stage output becomes the VCV (Voltage Control Voltage) output to the variable current sources and the high-frequency compensation circuit. The E10 to E11 connection, which allows the auxiliary board to modify the frequency control voltage, is not used in the Wavetek 271. A simplified schematic of the VCG amplifier is shown in figure 4-9.

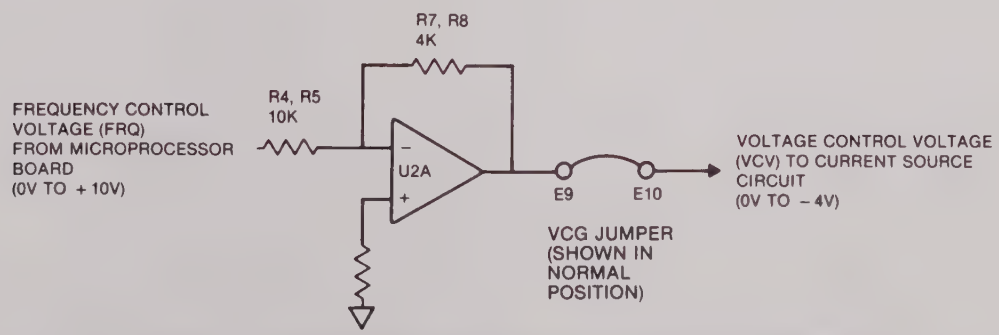


Figure 4-9. Simplified Schematic Diagram, VCG Amplifier

The current sources operate on the following principles:

1. The collector current of a transistor depends on its base current and its current gain, and is relatively independent of collector load resistance.
2. The base drive of a transistor can be adjusted to provide a known reference current in a known resistance in its collector circuit.
3. This same base drive, applied to a second matched transistor, will cause the second transistor to have the same collector current as the first transistor.

The negative current source is shown in the figure 4-10 simplified schematic diagram. The Voltage Control Voltage (VCV) is inverted by operational amplifier U2C, and drives transistor U3A to whatever value collector current is required to cause the U3A collector voltage to be equal to VCV. (At this point, both inputs of operational amplifier U2C are at the same voltage, and equilibrium is established.) Since the upper end of collector resistor R22D is held at ground potential (as will be explained later) and the voltage at the lower end is equal to VCV, the current through the resistor ($-I_{ref}$) is proportional to VCV. The same base drive is applied to U3B to generate the negative current source ($-I$), and is also applied to transistors U3C and Q1 to generate the Trigger Holding Current (THC).

The positive current source (shown in simplified schematic figure 4-11) operates in a similar manner, and tracks the negative current source. Operational amplifier U2D drives transistor U3E to whatever value collector current is required to maintain a "virtual ground" at the junction of R22C and R22D. Since these two resistors are in series, their currents are equal ($+I_{ref} = -I_{ref}$). The U3E base drive is then applied to matched transistor U3D to generate the positive current source ($+I$) for the generator loop.

The current source circuit also generates a Trigger Holding Current (THC) which is used to clamp the triangle node at ground potential during the "off" state in the gated and triggered modes. The circuit is shown in simplified schematic diagram figure 4-12.

The same transistor base drive that creates the negative current source ($-I$) is also applied to transistors U3C and Q1, driving each transistor to a collector current equal to $-I$. The two collectors are connected in parallel to provide a current equal to twice the $-I$ current source. This $-2I$ current is supplied by CR14 in the trigger circuit while the generator is gated "on".

When the generator is gated "off", a negative voltage is applied to the CR14 anode. This transition always occurs at the negative peak of the triangle waveform, and the $-2I$ current is momentarily supplied by CR7.

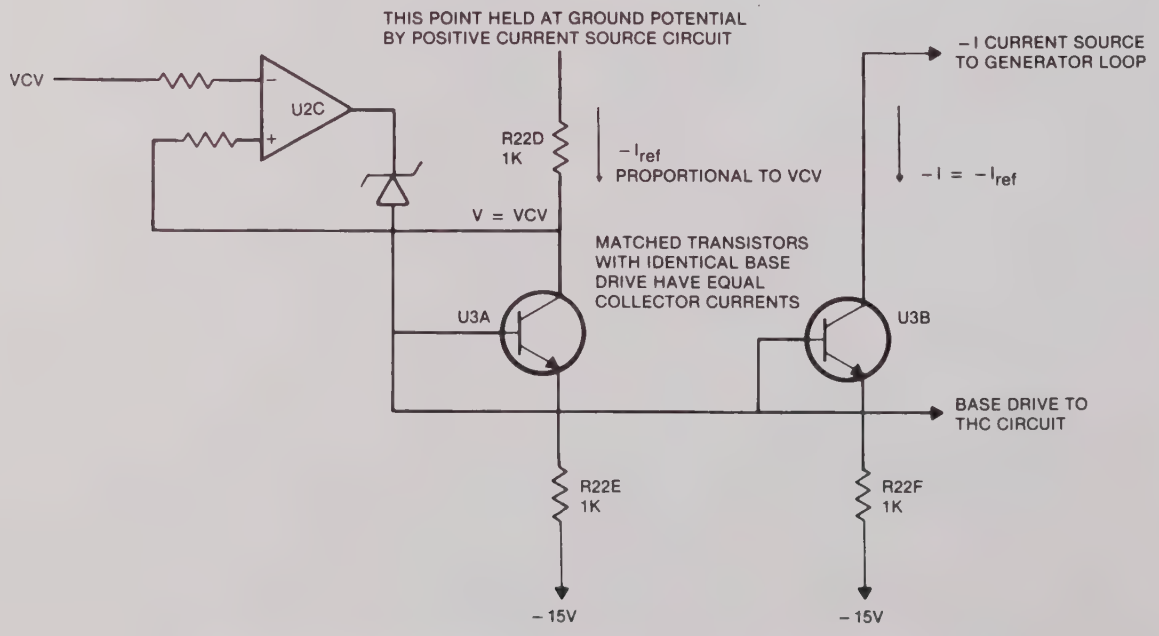


Figure 4-10. Simplified Schematic Diagram, Negative Current Source

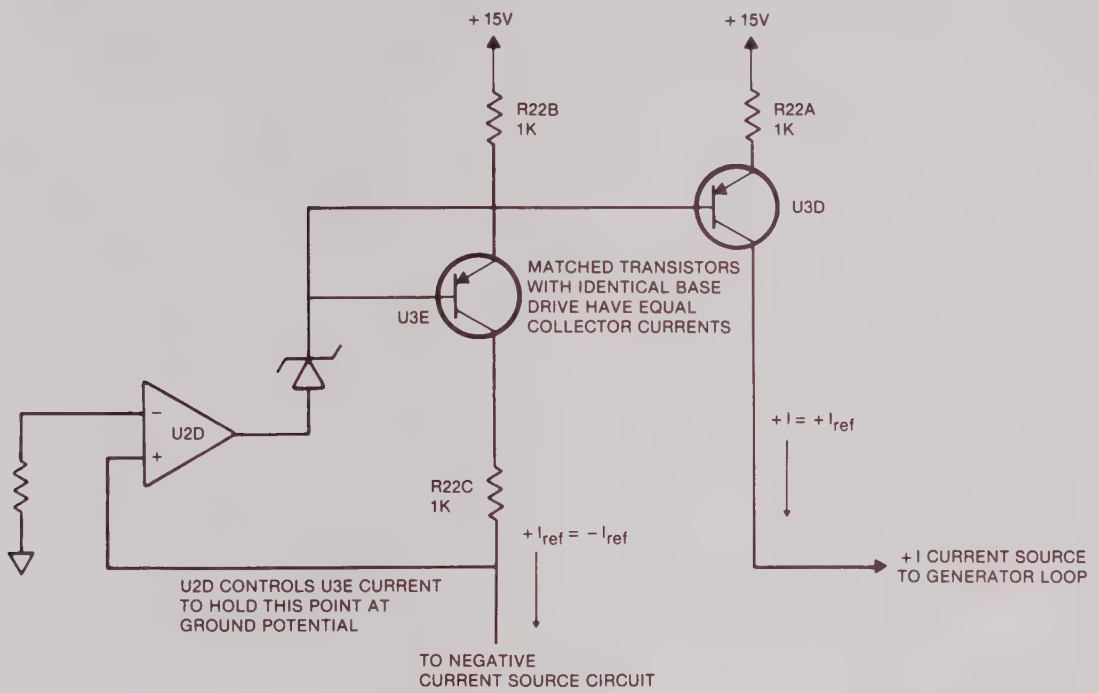


Figure 4-11. Simplified Schematic Diagram, Positive Current Source

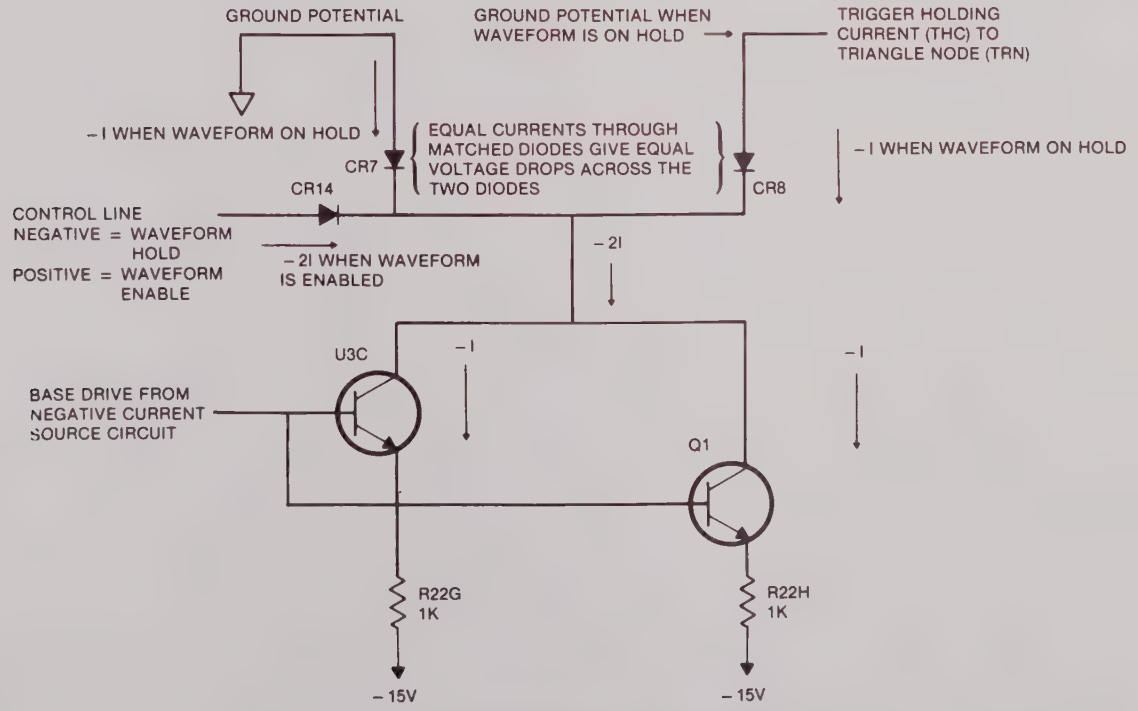


Figure 4-12. Simplified Schematic Diagram, THC Circuit

As the triangle node rises toward ground potential, a greater proportion of the −2I current flows through CR8. Equilibrium is reached when the trigger holding current is equal to the positive current (+I) being supplied to the generator loop, and the triangle node voltage cannot rise any further. Since the matched diodes CR7 and CR8 have equal currents through them and the anode of CR7 is grounded, the voltage drops across the two diodes will also be equal and the triangle node will be held at ground potential. This stops the waveform smoothly at the leading edge and ensures that at least one complete cycle will be generated every time the generator is triggered.

R23 adjusts the positive current source to precisely match the negative current and therefore maintain waveform symmetry. R12, which adjusts the low end frequency, sets the offset of the positive current amplifier, U2D, to match the offset of the negative current amplifier, U2C. R15 adds or subtracts current through the reference string to balance symmetry at low currents. The 8.2V zener diodes, CR4 and CR6, allow U3 pins 14 and 1 to approach the positive and negative supply rails respectively. Diodes CR3 and CR5 prevent latch-up.

The trigger level amplifier consists of an operational amplifier (U2B) in an inverting configuration that translates the trigger level control voltage from the microprocessor board (TRL, 0 to +10V) to the level used at the trigger comparator (TLO, +10 to −10V).

4.4.2 Generator Loop

The Generator Loop, shown in simplified schematic figure 4-13, produces simultaneous square and triangular waveforms. The triangular waveform is generated by alternately charging and discharging a timing capacitor from adjustable constant-current sources. The value of the selected timing capacitor determines the frequency range of the loop. Within any range, frequency is determined by the magnitude of the +I and

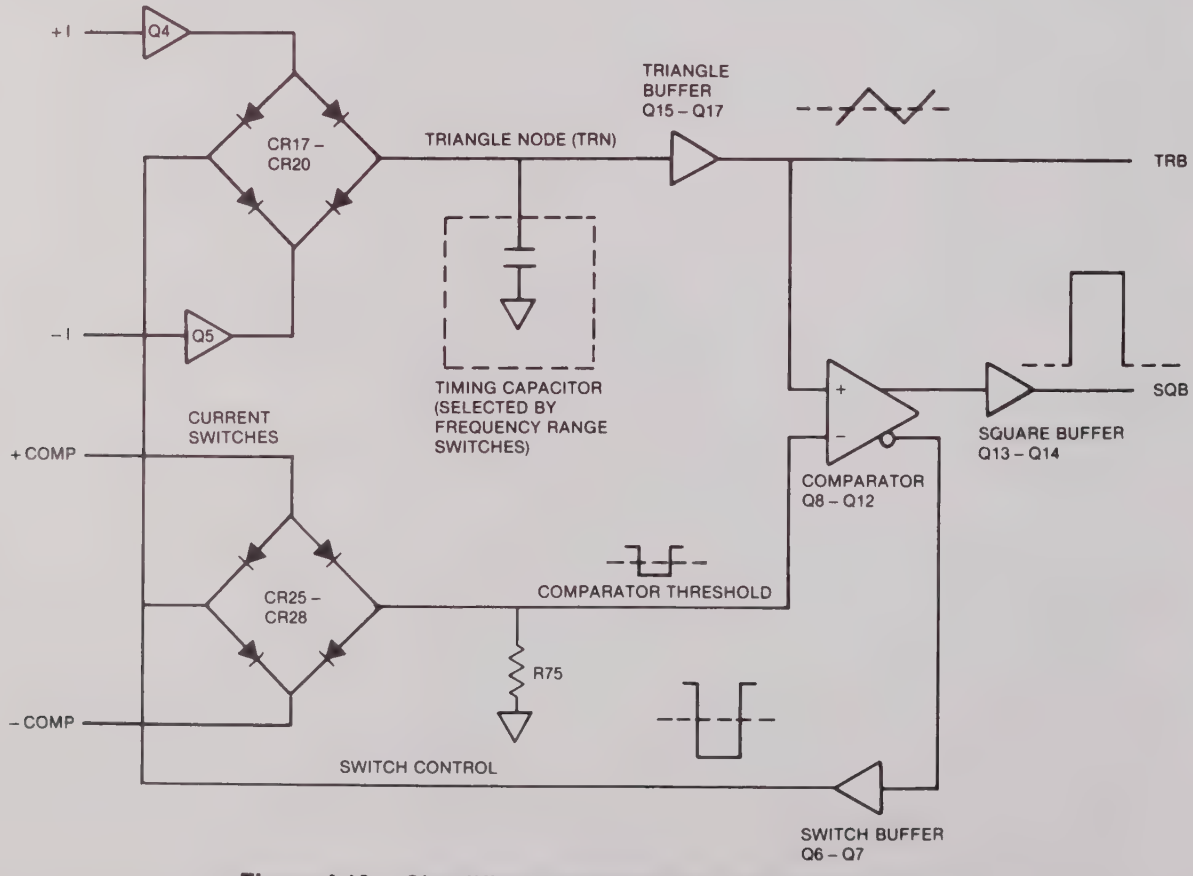


Figure 4-13. Simplified Schematic Diagram, Generator Loop

– I currents from the VCG circuit. Charging the capacitor from a current source gives a linear voltage change with respect to time, instead of the exponential curve that would result if a resistor were used.

The comparator monitors the amplitude of the triangle wave, and when it reaches the comparator threshold, the comparator changes states. The state of the comparator output determines the polarity of the comparator threshold and the direction of the capacitor charge/discharge current. The comparator output is also used to generate the square wave output.

Magnitude of the comparator threshold is determined by the value of the + COMP and – COMP currents from the high frequency compensation circuit. The positive or negative current selected by current switch CR25-CR28 flows through R75, and the voltage drop across R75 becomes the comparator threshold voltage. The high frequency compensation circuit reduces the + COMP and – COMP currents on the three highest frequency ranges to reduce the comparator threshold voltage to compensate for switching delays.

Operation of the diode current switch is illustrated in simplified schematic diagram figure 4-14. In this simplified schematic, voltage drops across the forward-biased diodes are assumed to be 0.6 volts, and the voltages shown are not intended to represent exact circuit voltages. Although this diagram shows the CR17-CR20 current switch, the same principles of operation also apply to the CR25-CR28 circuit.

The current switch has three inputs and one output. The inputs are the positive and negative currents (buffered by Q4 and Q5) and the control voltage; the output is the switched current. The magnitude of the control voltage must be greater than the voltage at the output that is caused by the switched current flowing through the external load. In this example, voltage at the triangle node (TRN) will not exceed ± 1V before the comparator changes states and causes the voltage to move in the opposite direction.

With the control input at + 2V, CR18 and CR19 are reverse biased. Current flows from the + I source through CR17 into the timing capacitor, and from the control line through CR20 into the negative current source. With the control line input at – 2V, CR17 and CR20 are reverse biased. Current flow is from the + I source

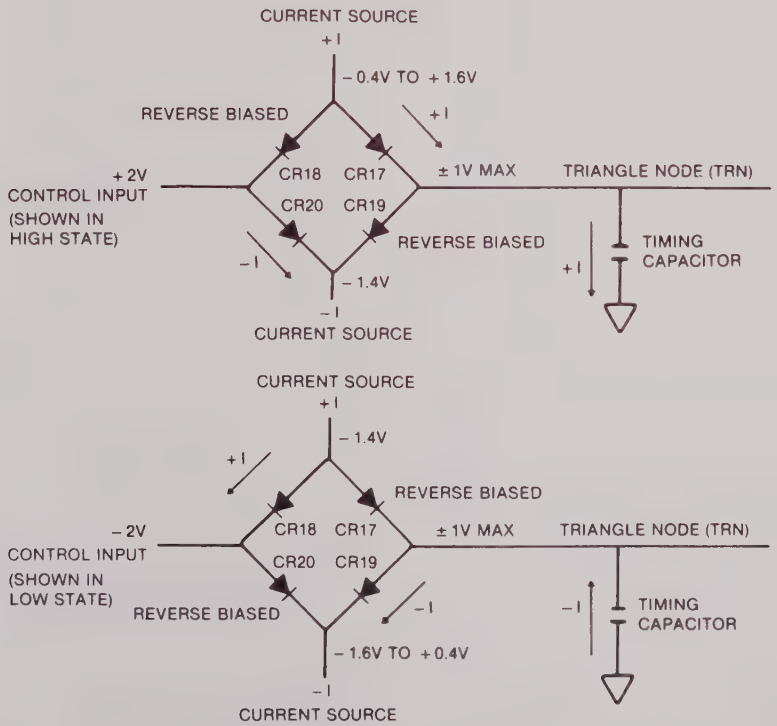


Figure 4-14. Simplified Schematic Diagram, Current Switch

through CR18 into the control line, and from the timing capacitor through CR19 to the −I source.

The CR25-CR28 current switch operates in a similar manner. Voltage at the output of this switch is limited to ±1V by the 3 mA maximum value of the current and the 332Ω resistance of R75.

For the remainder of the circuit description of the Generator Loop, refer to the complete schematic diagram.

The comparator is made up of current source Q10, differential pair Q9 and Q11, and a second differential pair, Q8 and Q12. As the rising ramp of the triangle wave at the base of Q11 reaches the positive reference level (+1V) at the base of Q9, Q11 of the differential pair turns on as Q9 turns off. CR29 and CR30 increase the transistor switching speed by limiting the signal swing at the collectors of Q9 and Q11 to about 0.7V. As Q9 and Q11 switch, they also cause the second differential pair, Q8 and Q12, to switch. Resistors R72 and R84 increase the switching speed of Q8 and Q12 respectively by providing a small current which keeps them from turning entirely off. As Q8 switches to its relatively "off" state, current through R73 decreases and the collector of Q8 falls to its low state, about −1.6V, determined by the current drain through R71. The collector of Q8 drives the switch buffer; the square buffer is driven by Q12 in the opposite side of the comparator. These two stages have different values of collector and emitter resistors to match the output requirements of the associated buffers.

The switch buffer (Q6-Q7) is a push-pull emitter follower biased on by the voltage drops across CR22 and CR23. The output is a ±2.2V square wave that drives the two current switches in the generator loop.

The square buffer (Q13-Q14) is similar to the switch buffer circuit, except that resistor values are tailored for a 0 to +5V output. This signal, SQB, is used to drive the sync driver and trigger circuits. The SQB signal is attenuated by R100 and R101 to provide the SQS signal used by the square logic and the pulse board. A highly differentiated portion of the SQB transient is coupled through C35, C36 and C27 to the triangle node to counteract switching transients which are coupled through the current switch diode bridge.

The alternating linear ramp (triangle wave) at the triangle node is buffered by the triangle buffer, a high speed FET input voltage follower. This circuit consists of Q15, acting as a source follower, and Q16, acting as an emitter follower. The voltage difference between the input and output of the circuit is controlled by maintaining the current through Q15 so that the gate-source voltage is equal and opposite to the base-emitter drop of Q16 and the two voltages cancel each other. The current through Q15 is initially set by adjusting R99, the NODE DC adjustment after which the dc amplifier in the frequency compensation circuit maintains this adjustment through the constant current source, Q17, to compensate for temperature changes in Q15.

4.4.3 Frequency Range Switches

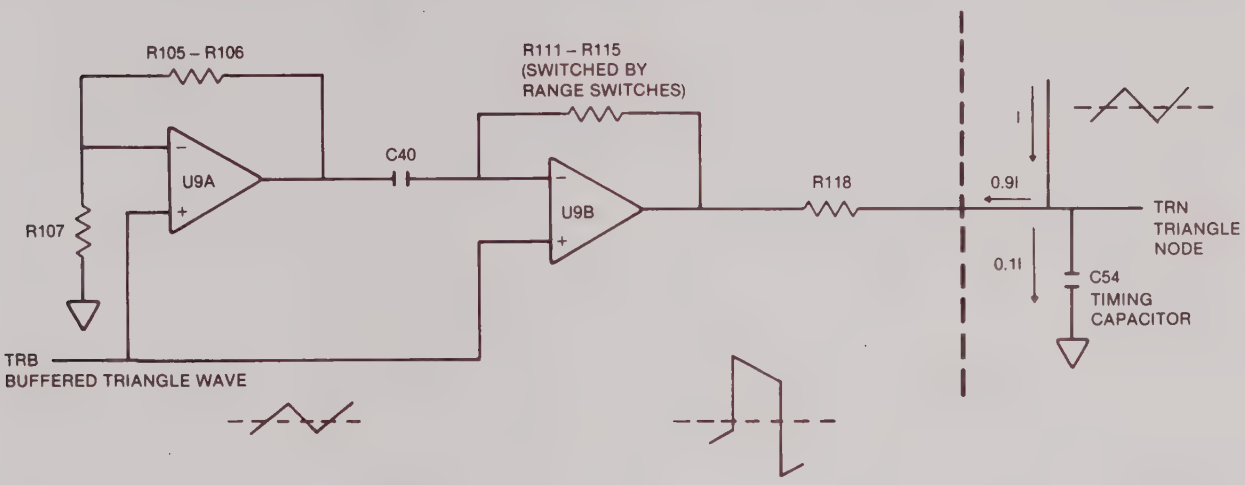
The selected range capacitor determines the frequency range from 100 Hz to 12 MHz. Each range normally covers 10% to 99.9% of full scale. Capacitance for the highest frequency range consists of all the stray capacitance on the triangle node added to C43 (the 1 MHz adjustment capacitor) and C44, which brings the total to 100 pF. The next range switches in an additional 900 pF, made up of C46, C47 and the 100 kHz adjustment C45. The next three ranges switch in successive matched capacitors of 0.01μF (C50), 0.1μF (C52) and 1.0μF (C54).

Each range capacitor is switched in by a logic level signal from the microprocessor board. For example, when $\overline{FR6}$ (Frequency Range from 0.1 MHz to 1 MHz) goes low, it turns on Q18, which sources about 30 mA through R124 and diodes CR36 and CR37. When CR37 is forward biased with this amount of current, its impedance to ground is less than 2Ω, and the range capacitor made up of C45, C46 and C47 is effectively connected to ground. When this range is not selected, $\overline{FR6}$ is high, turning off Q18 and allowing R125 to pull the anode of CR36 to −15V. The voltage divider, R121 and R122, pulls the anode of CR37 to −7.5V through the 10 MΩ resistor R123. Reverse-biased CR37 now provides an essentially infinite impedance, effectively disconnecting the range capacitor. The other range switches operate in exactly the same way.

4.4.4 Capacitance Multiplier

The capacitance multiplier extends the low end frequency range by drawing off (through R118) most of the charging current to and from the largest range capacitor, C54. The circuit is shown in simplified form in figure 4-15. The U9B output waveform is a triangle wave superimposed on a square wave. The square wave component determines the polarity of the voltage across R118, and therefore the *direction* of current flow through this resistor. The triangle component maintains the *magnitude* of the R118 voltage and current constant to maintain linearity of the triangle node waveform.

The square wave component is generated by differentiating the triangle wave. The triangle wave is amplified by U9A, then differentiated by C40 and U9B. U9B also sums the triangle wave at its non-inverting input with the square wave. The resulting output is applied to the triangle node through R118.



NOTES:

1. Direction of currents shown is for capacitor charging in positive direction.
2. Ratio of capacitor current to total current depends on frequency range selected.

Figure 4-15. Simplified Schematic Diagram, Capacitance Multiplier

The capacitance multiplier is switched in at frequencies below 100 Hz by a logic low on the $\overline{\text{CPM}}$ control line. The proportion of capacitor charging current is determined by the range resistors. $\overline{\text{FR2}}$ selects R111 (plus the 99.9 Hz adjust, R112) and decreases the capacitor charging current to 10% of its normal value. Each successive decade of added resistance decreases the capacitor current to 10% of its previous range. R105 adjusts the overall calibration of the capacitance multiplier by adjusting the gain of the first amplifier, and R117 adjusts the capacitance multiplier symmetry by adjusting the offset of the second amplifier.

4.4.5 Frequency Compensation

The Frequency Compensation circuit contains the high frequency compensation, which reduces the Generator Loop comparator threshold on the three highest frequency ranges to compensate for comparator switching delays, and the dc amplifier circuit, which dynamically controls the dc offset in the triangle buffer.

The high frequency compensation circuit is shown in simplified schematic diagram figure 4-16. This circuit generates the two adjustable constant currents (+COMP and −COMP) that alternately flow through R75 in the comparator circuit in the Generator Loop to develop the comparator threshold voltages. On the lower frequency ranges, these currents each have a fixed value of 3 mA. On the three highest ranges, the currents are reduced in proportion to both the range selected and the programmed frequency within the range.

On the lower frequency ranges, the range switches are all open, and voltage divider R53, R50, R52 develops a voltage of +7.5V at the junction of R53 and R50. This voltage is applied to the non-inverting input of operational amplifier U7B, which drives the source of Q2 (and the inverting input of U7B) to the same voltage. The resulting +7.5V at the junction of R56 and R54 causes a current of 3.75 mA in R56 and 0.75 mA in R54. The difference of these two currents is the 3 mA +COMP current.

U7A and Q3 track the positive current source to generate a negative current (−COMP) of equal magnitude. U7A monitors the voltage at the midpoint of R54 and R57, which are connected in series between the source of Q2 and the source of Q3. As U7A acts to keep its two inputs at equal voltages (and the midpoint of the resistors at ground potential) it drives the Q3 source to a voltage equal in magnitude and opposite in polarity to the voltage at the Q2 source. The Q3 source voltage determines the currents in R57 and the series combination of R59 and R60. The difference of these two currents is the 3 mA −COMP current.

Operational amplifier U7C converts the negative Voltage Control Voltage (VCV) to a voltage that is positive in proportion (within any frequency range) to the programmed

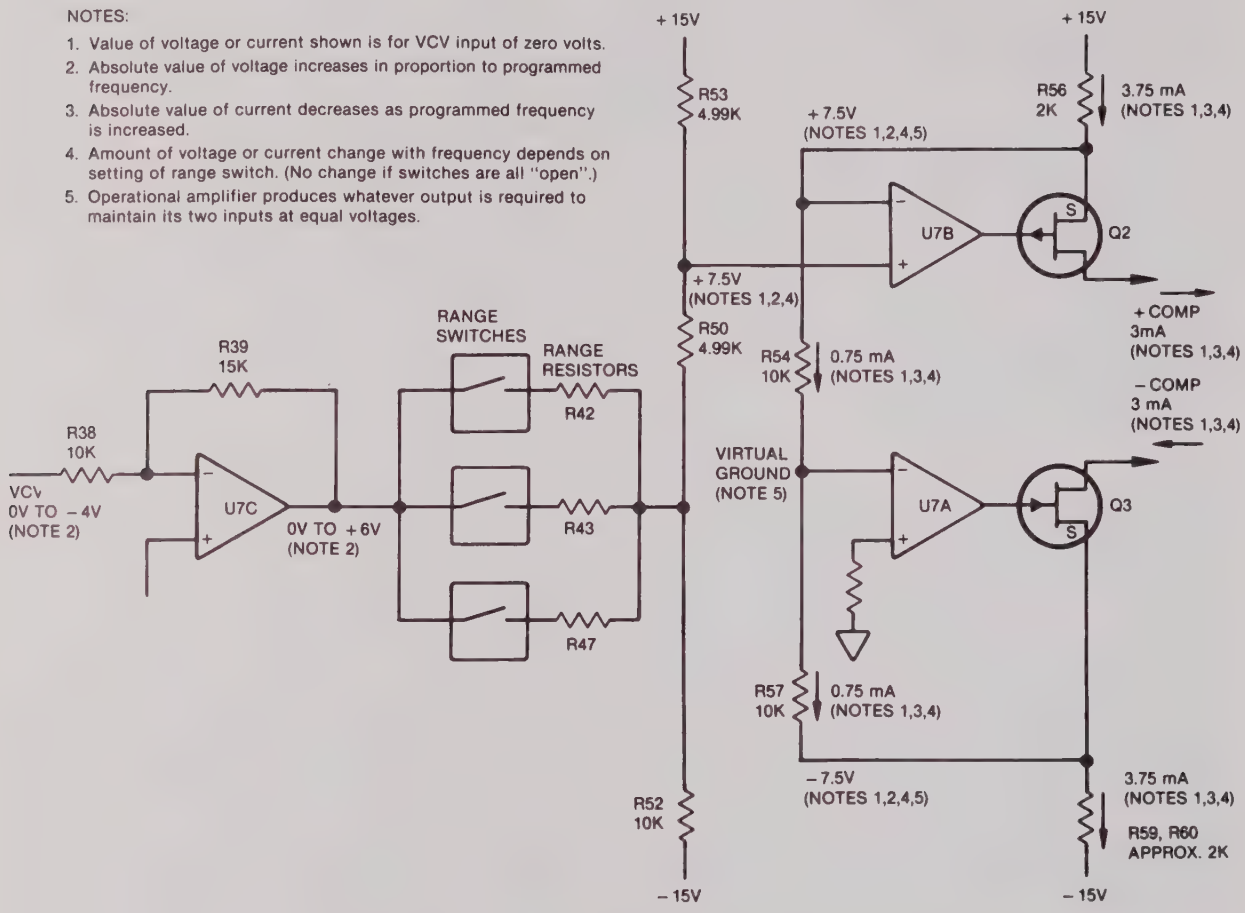


Figure 4-16. Simplified Schematic Diagram, High Frequency Compensation

frequency. Although the range of this voltage is 0V to +6V, it will normally be above +0.6V except at the bottom end of the lowest frequency range. On the top three frequency ranges, one of the solid-state range switches is closed by a logic low on its control line, connecting this voltage through one of the range resistors (R42, R43 or R47) to the R53, R50, R52 voltage divider. This raises the voltage at the junction of R53 and R50, causing the absolute values of the Q2 and Q3 source voltages to increase and the source currents to decrease. The result is a decrease in the +COMP and −COMP currents proportional to both frequency range and programmed frequency within the range.

R44 causes a small voltage change in the output currents proportional to VCV to compensate for a small nonlinearity in frequency tracking. R60 balances the triangle waveform, while R45 and R46 allow adjustment of frequency on the top two frequency ranges. Zener diodes CR15 and CR16 (not shown on the simplified schematic) act as level shifters to allow the operational amplifier outputs to operate near ground potential while the gates of Q2 and Q3 operate closer to the supply voltages.

The dc amplifier keeps the output of the triangle buffer at the same dc level as the input by varying the current through the constant current source, Q17, and therefore through the input FET, Q15. It does this by comparing highly filtered signals at the operational amplifier inputs, U7D pins 12 and 13, and varying the current through R104 to compensate for errors. Below 100 Hz, $\overline{\text{DCA}}$ switches out filter capacitors C17 and C58; this allows U7D pin 14 direct control of the current through R104, thus giving greater accuracy.

4.4.6 Sync Driver

The Sync Driver is a double emitter follower that buffers the generator loop's square output, SQB, to provide a synchronizing signal for the instrument.

Transistors Q26 and Q27 are biased on by the voltage drop across CR52 and CR53. R171 and R175 provide about 4 mA through the diodes, and resistors R173, R181 and R183 balance the current so the transistors also have about 4 mA through them. The small emitter resistors also prevent thermal runaway. Collector resistors protect the transistors from overvoltage at the output connector, and capacitors C70 and C71 prevent large signal swings at high frequencies that would reduce the gain of the transistors and add noise to the circuit.

4.4.7 Trigger Circuit

The trigger circuit allows the instrument user to trigger or gate the generator from an external signal of widely varying characteristics with a fixed and stable delay between the trigger source and the resultant generator output.

Trigger comparator U4 compares the level of the trigger input with the reference level (TLO) programmed in the generator. The comparator output goes to a logic low at U4 pin 9 if the trigger input becomes greater than the reference level and positive trigger slope (+TR) has been selected, or it goes to a logic low at U4 pin 11 if the trigger input becomes less than the reference level and negative trigger slope (−TR) has been programmed. A logic low transition at either comparator output will cause a logic high at the pin 8 output of NAND gate U5C; this positive-going transition clocks the remainder of the trigger logic. (When the instrument is manually triggered from either the front panel or the GPIB, the microprocessor sets both the +TR and −TR lines high to cause an unconditional logic high at the output of U5C.)

In the Wavetek 271 the output of the trigger comparator at U5C is always routed through the pulse board, and the TRIG JUMPER is connected from E13 to E14. This jumper must *never* be connected from E12 to E13, as this will place the output of NAND gate U5C on the function generator board in parallel with the output of U8B on the pulse board.

Refer to Figure 4-17, Simplified Schematic Diagram, Trigger Circuit Mode Logic, for the following discussion. The trigger circuit is enabled by a logic high on the MC0 line. Selection of triggered or gated mode is performed by logic line MC1; the line is low for triggered mode or high for gated mode.

In the triggered mode, only one cycle of generator output is enabled for each trigger pulse applied. A logic low on mode control line MC1 disables NAND gate U5D. The high level on the output of U5D disables the direct $\overline{SET}$ input of flip-flop U6B and enables NAND gate U5B. A positive logic transition at trigger jumper terminal E13 clocks flip-flop U6B to the "set" condition, causing the $\overline{Q}$ output to go low. This low is applied to the direct $\overline{CLEAR}$ input of U6A, giving a logic low at the U6A Q output. The low at U6A-Q causes a high at the output of NAND gate U5A, reverse biasing diode CR8 and allowing the generator loop to oscillate. The first positive transition of SQB, 90° later on the triangle waveform, is inverted by NAND gate U5B and applied to the $\overline{CLEAR}$ input of U6B to clear the $\overline{Q}$ output high, thereby removing the low from the $\overline{CLEAR}$ input of U6A. The next negative transition of SQB is inverted by U5B, and clocks U6A to the "set" condition. The high at U6A-Q causes the output

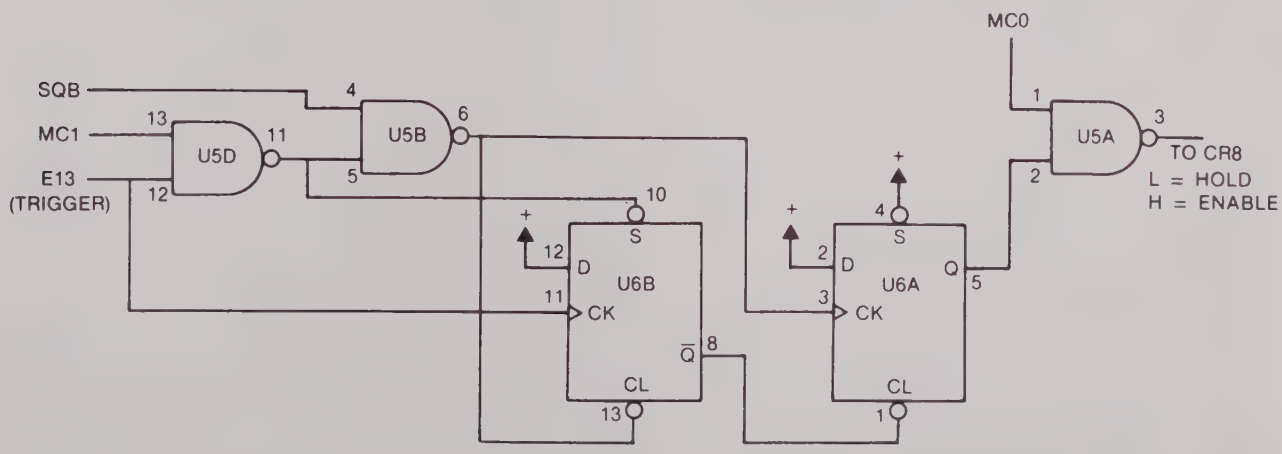


Figure 4-17. Simplified Trigger Circuit Mode Logic Schematic Diagram

of gate U5A to go low, forward biasing diode CR8 and stopping the triangle oscillation on its rising edge.

In the gated mode, the generator output is continuously enabled for the entire duration of the applied trigger signal. A logic high on mode control line MC1 enables NAND gate U5D, causing the U5D output to be low whenever the E13 trigger level is high. Operation in the gated mode is the same as in the triggered mode except that during the time that the E13 trigger level is high, the resulting low at the U5D output will:

1. Hold flip-flop U6B in the "set" condition via the direct $\overline{\text{SET}}$ input.
2. Disable NAND gate U5B, preventing the SQB signal from clearing U6B and clocking U6A until after the trigger signal is removed.

Resistors R29, R303, R34, R31 and R32 divide the reference (TLO) and input (TRIG IN) voltages by a factor of 4 to bring them within range of the U4 comparator. Diodes CR9, CR10 and CR11 protect the U4 comparator from excessive voltage at the trigger input. Resistors R33 and R35 provide a small amount of hysteresis at the U4 comparator input to prevent false triggering on noise.

4.4.8 Function Select

The function select circuit connects the sine, triangle or square (all disconnected in dc function) to the current input of the X-Y multiplier.

The sine wave input is created from the triangle buffer output, TRB, by the sine converter which uses the logarithmic response characteristics of semiconductors diodes to approximate a sine wave current output. The SIN DIST A adjustment, R142, adjusts the converter input for diode forward voltage variation. The six diodes in U11 give a three stage sine approximation using very closely matched characteristics of the diodes. Two adjustments, SIN DIST B and SIN DIST C (R154 and R157), balance between stages for positive and negative peaks respectively. The current output is switched through FET switch U12A when $\overline{\text{SIN}}$ is selected.

The triangle level control (R148), provides an adjustable current to FET switch, U12C controlled by $\overline{\text{TRI}}$. Both the triangle and sine FET switches provide increased isolation by shorting the FET switch input (with Q25 and Q22 respectively) when the switch is off.

The square logic selects which rectangular waveform is fed to the square shaper. A logic high on the SQR control line selects the uninverted SQS square wave, while a high on the $\overline{\text{SQR}}$ line selects the SQS signal after it has been inverted by U13C. A logic high on the external width control line (EXW) selects the output of the trigger circuit, TRGI. Control lines PLS and $\overline{\text{PLS}}$ select the normal or inverted input (PLSI) from the pulse board.

The square shaper converts the TTL level signal at U13A pin 3 to ± 1 mA. It shifts the TTL signal and uses it to switch current sources through a diode switch (CR48 through CR51) and into the FET switch U12D (controlled by $\overline{\text{RCT}}$). The current sources for upper and lower levels of square waves are independently adjustable by R164 and R168 respectively.

4.4.9 X-Y Multiplier and Offset

4.4.9.1 X-Y Multiplier

The X-Y multiplier is a precision voltage-controlled amplifier that drives the preamplifier with a signal level directly proportional to the amplitude control voltage (AMP) from the microprocessor board.

As shown in the figure 4-18 block diagram, the X-Y multiplier consists of five major circuit groups: Logarithmic signal compressor, variable gain signal amplifier, logarithmic dc reference, variable gain reference amplifier, and dc amplifiers. The input signal (XYI) is logarithmically compressed in U18A, then amplified by variable gain signal amplifier U19A. Because the control voltage vs. gain characteristic of the variable gain amplifier is not linear, the remainder of the circuit is required to convert the input amplitude control voltage (AMP) to a modified gain control voltage.

U18B generates a dc reference voltage proportional to the logarithm of the difference of two currents. This reference voltage is amplified by variable gain reference amplifier U19B and fixed gain dc amplifiers U17A and U17D, then compared to the amplitude control voltage (AMP) by U17B. U17B provides the modified gain control voltage to both variable gain amplifiers, and adjusts the gain of the reference amplifier upwards or downwards as required until the amplified reference voltage is equal to the input amplitude control voltage (AMP). The same modified gain control voltage that controls the gain of the variable gain reference amplifier is also applied to the variable gain signal amplifier.

The logarithmic signal compressor (U18A) consists of a differential transistor pair connected as diodes. One side of the differential pair is connected to ground, the other side to the XYI signal input. Each side of the differential pair is biased to about 3 mA (the optimum diode current for logarithmic compression) by the current source transistor within the IC. The input signal current (± 1 mA) on the XYI line causes a small ac voltage across the diode that varies approximately as the logarithm of the total current. This voltage also drives one base of the output differential pair (U19 pin 2), while the other base is approximately at ground potential, adjusted by the multiplier distortion adjustment, R255. The current source transistor in the output stage (U19 pin 3) is driven

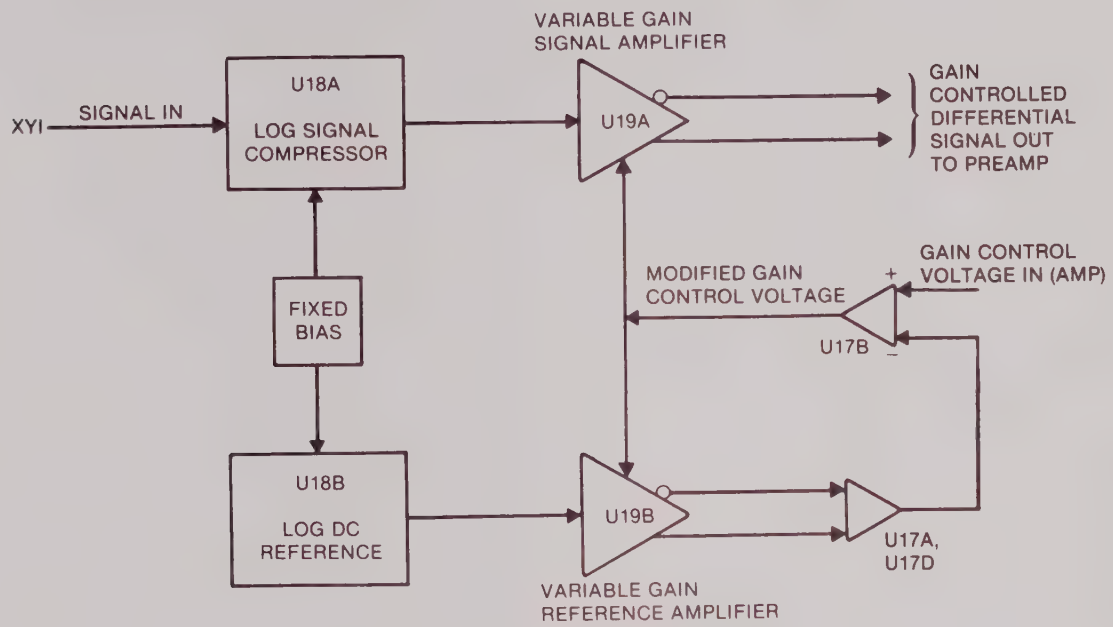


Figure 4-18. X-Y Multiplier Block Diagram

by the modified gain control voltage. Maximum output from the stage occurs with a maximum total bias current of 6 mA; less bias current produces less output.

The logarithmic dc reference (U18B) is configured much the same as the logarithmic signal compressor described above. Total bias current through the differential pair is fixed at 6 mA, but is unevenly split, with 4 mA through one side and 2 mA through the other side (limited by R242 and R243). This corresponds to the current ratio in the signal compressor during peaks of the signal, when the instantaneous peak signal current of 1 mA adds to the 3 mA dc current in one half of the differential pair and subtracts from the 3 mA dc current in the other half. The dc reference voltage is taken from U18 base and collector terminals 8 and 9.

A simplified schematic diagram of the variable gain reference amplifier and associated dc amplifiers is shown in figure 4-19. The input amplitude control voltage (AMP) drives U17B (pin 5), which in turn drives the base (pin 11) of the current source transistor in U19B. The base of one side of the differential pair (U19 pin 9) is connected to ground through a resistor; the base of the other side of the pair (U19 pin 6) is connected to the log dc reference voltage. These base voltages will maintain the currents in the differential pair in the ratio 1:2 regardless of total current flow determined by the current source transistor. The collectors of the differential pair are connected to the inverting inputs of operational amplifiers U17D and U17A (pins 13 and 2). These inverting inputs are "virtual grounds"; because the non-inverting inputs of these amplifiers are grounded, each amplifier will provide whatever output level is required to keep its two inputs at the same voltage level. The value of resistors R256 through R258 were chosen so that with 6 mA through the current source transistor in U19B:

1. 2 mA flows through R256 from U17D pin 17 to U19B pin 7.
2. 2 mA flows through R257 from U17D pin 14 to U19B pin 8.
3. An additional 2 mA flows from U17A pin 1 through R258 to U19B pin 8.
4. The voltage at the output of U17A (pin 1) is 10 Vdc, which exactly equals the 10 Vdc external AMP input, maintaining the inputs of U17B (pins 5 and 6) at equal voltages.

With input amplitude control voltage (AMP) less than 10V, all voltages and currents in the circuit are proportionately less.

The output of the circuit is the modified gain control voltage at the output of U17B (pin 7). This voltage is used to control the variable gain signal amplifier.

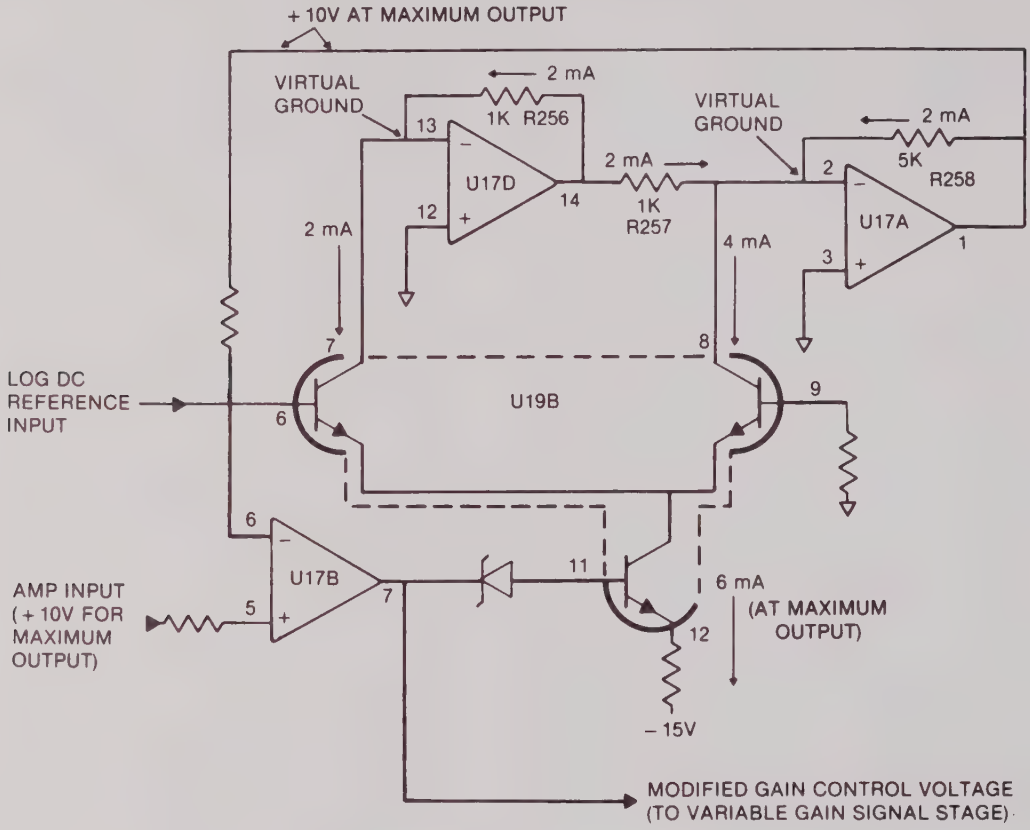


Figure 4-19. Variable Gain Reference Amplifier

Fixed bias for both sections of U18 is provided by R248, CR59 and CR60. CR61 performs a level shifting function, allowing the base terminals of U19 (pins 3 and 11) to operate near the negative supply voltage while the output of U17 (pin 7) operates closer to ground potential.

The X-Y multiplier circuit contains four calibration adjustments: R241, R242, R251 and R255. Adjustment procedure for these controls is given in the CALIBRATION section of the manual.

4.4.9.2 Offset Circuit

The offset circuit is a level translator that converts the 0 to +10V input from the microprocessor board (OST) into a +5 to −5 Vdc signal that sums into the output amplifier. Any offset caused by the operational amplifier at U17C pin 8 is corrected by the offset zero adjustment, R237. The output of the amplifier is then adjusted for dc offset by the offset adjust, R208.

4.4.10 Preamplifier

The preamplifier takes the differential current output of the X-Y multiplier from U19 pins 1 and 14 and converts it to a single-ended voltage output at the anode of CR54. The voltage at the inputs of the differential stage (U15 pins 3 and 16) must be maintained at about +0.7 volts to bias the input transistors whose emitters are at ground. The emitter of the transistor at U15 pin 8 provides the current to maintain this voltage. The current can be as high as 6 mA or as low as 0.06 mA, depending on the current required by the output stage of the X-Y multiplier. Added to this current is the bias current for the preamplifier itself, about 1 mA each through the feedback resistor strings consisting of the 750Ω, 0.1% resistors R189 and R192, and R194 and R198. The full-scale current output of the X-Y multiplier is ±1 mA in each leg of the output differential stage, and this current is translated into a ±0.75 Vac signal at U15-8 and a ±1.5 Vac signal of the opposite phase at the CR54

anode. PNP transistors Q28 and Q29 act as constant current sources for the input stage collectors (U15-2 and U15-1 respectively) and they also act as an ac bootstrap through coupling capacitors C76 and C79. The emitter follower stages, U15-8 and U15-11, isolate the collectors of the input stages to provide a low impedance output.

4.4.11 Output Amplifier

The output amplifier is an inverting and summing amplifier with a gain of about −6.67 for the ac signal from the preamplifier. The amplifier operates differently for high-frequency signals than for low-frequency signals; high-frequency signals couple into the symmetric emitter followers Q30 and Q31 through capacitors C90 and C91 respectively. The emitter followers then drive the symmetrical inverter stage consisting of Q32 and Q33. Diodes CR55 and CR56, with the 10Ω resistor, R219, provide a bias current through the output stage of Q34, Q35, Q36 and Q37 to increase output speed by keeping the transistors always on. The 10Ω emitter resistors, R227, R228, R231 and R232, balance the current through the parallel output stage transistors to improve their power handling capability. The output signal (+ and − 10V, maximum) is fed back through resistors R223 and R217 in series to the input. The trim capacitors, C97 (output amplifier peaking) and C122 (output amplifier roll-off), adjust the amplifier high speed characteristics by rolling off or peaking the feedback signal respectively.

The low-frequency (and dc) path in the output amplifier is through the transistor array, U16, connected as an operational amplifier. The positive output of the differential input stage (U16-3) is inverted at U16-9. This signal decreases the current through transistor Q32 and the signal at its collector falls until the fed back signal balances the input, either ac (through R207) or offset (through R208 and R209). The PNP transistors in U16 balance the current through the differential input pair and provide a high impedance load for the first stage output. Capacitor C86 decreases the speed of the low-frequency section at high frequencies.

4.4.12 Output Protection and Attenuator

There are three output amplifier protection safeguards to protect this circuit against major damage under the severest accidental misuse, including accidental connection of line power to the FUNC OUT connector. These safeguards are:

1. An overvoltage sensing circuit that detects voltages that exceed the ± 15V limits at the FUNC OUT connector. When an overload is detected, the circuit opens all relays in the output attenuator circuits and disconnects the amplifier from FUNC OUT.
2. An in-line fuse to protect the amplifier in case the voltage is great enough to arc across the relay contacts. Should the fuse blow, a sensing circuit alerts the microprocessor.
3. Two voltage-limiting, high current diodes (CR57 and CR58) at the amplifier output that prevent an externally applied voltage from pulling the amplifier output line beyond the range of the ± 15V supplies.

4.4.12.1 Overvoltage Sense Circuit

The overvoltage sense circuit compares the voltage at FUNC OUT (through isolating 1 MΩ resistors R298 and R299) with the ± 15V power supplies at U20 pin 4 and U20 pin 6 respectively. If the voltage at FUNC OUT goes higher than + 15V or lower than − 15V, the appropriate comparator output (U20 pin 2 or U20 pin 1 respectively) goes negative. Since the outputs are wire-ORed, when either output becomes negative it drives the comparator output at U20 pin 14 positive. This turns off Q38 and opens all relays to disconnect the amplifier from the output. The positive level at U20 pin 14 also signals the microprocessor (via the OAP line) that the output protection circuit has been activated. The microprocessor immediately signals the operator through the front panel display, the beeper and the GPIB. Removal of the external over- voltage immediately returns the output to its previous state and normal operation is resumed. The response of the relays is usually fast enough to prevent any damage whatsoever to the output amplifier with overvoltages up to 200 Vdc or 140 Vac.

4.4.12.2 Fuse Protection

Voltages greater than ± 200V may cause the relay contacts to arc and conduct. If such a condition occurs, a fast-acting fuse, F1, will generally blow soon enough to prevent, or at least minimize, damage to the instrument. A fuse sense circuit detects when the fuse is blown by pulling the output side of the fuse toward + 15V through 1 MΩ resistor, R288. If the fuse is open during power-up or reset (K1 off), the sense point rises higher than the amplifier output would normally let it go and the comparator output at U20-13 goes high if that voltage rises above + 13.6V. The microprocessor samples the logic levels at the fuse-blown indicator line (FUB) and signals the operator through the front panel display and the GPIB bus.

4.4.12.3 Output Attenuator

All three output relays (K1, K2 and K3) are independently driven by Q39, Q40 and Q41 and controlled by logic lines OA0 and OA2 from the microprocessor. OA0 determines

whether or not the output amplifier is connected, while OA2 switches the attenuator in or out. K2 and K3 both operate from the OA2 line, and operate opposite of each other (when one is on, the other is always off).

There are five possible combinations of operating states for the three relays. They are:

1. Overvoltage circuit tripped (Q38 turned off).
2. OUTPUT OFF (0) mode.
3. OUTPUT ON (1) mode, no attenuation. Output voltages (amplitude + offset) programmed for greater than 1.00V.
4. OUTPUT ON (1) mode, 20 dB attenuation. Output voltages (amplitude + offset) programmed for 1.00V or less.
5. OUTPUT OFF, LO Z (2) mode. Output terminated in approximately 50 ohms.

Relay states for these five conditions are shown in simplified schematic diagram Figure 4-20. In this figure, R289-R292 and R295 are shown as a single 50Ω resistor; R293, R294, R296 and R297 are shown as a single 55.6Ω resistor.

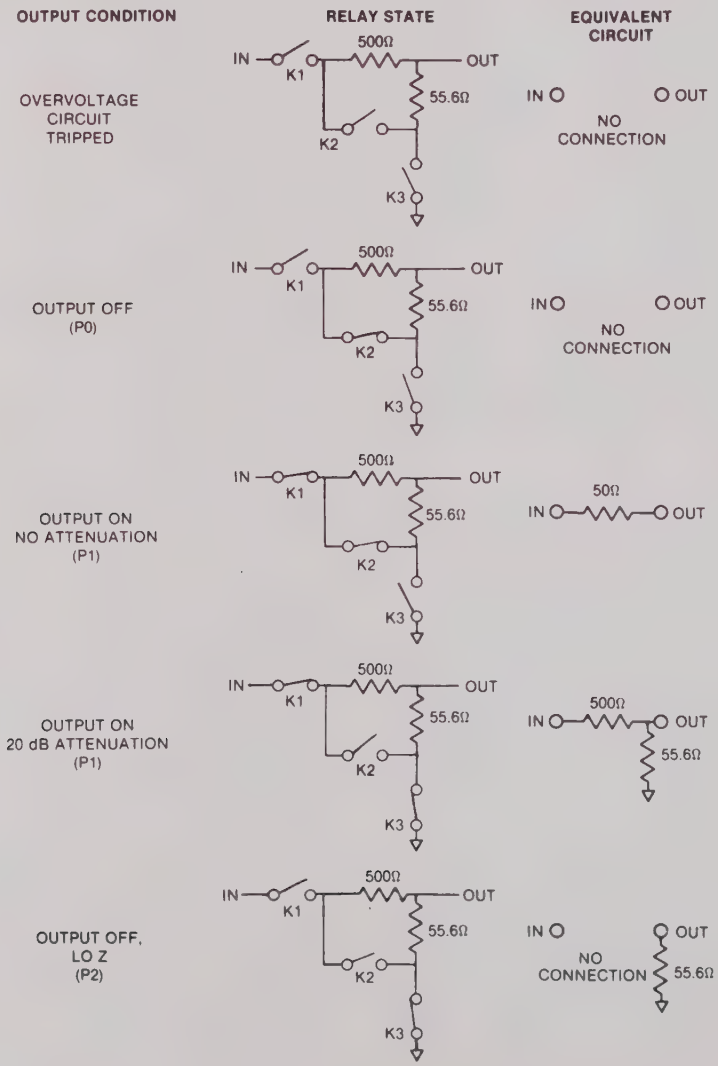


Figure 4-20. Output Attenuator Relay States

4.5 PULSE BOARD CIRCUIT DESCRIPTION

The pulse board contains four major functional circuit groups. These are:

1. The pulse generator, which creates pulses of selectable delay and width when the pulse mode is selected.
2. The burst counter, which enables the function generator output for a predetermined number of output cycles when the burst mode is selected and the circuit is triggered.
3. The control logic registers, which store data from the 8-bit data bus to drive 40 of the internal data and control lines.
4. The ±10 volt reference circuit, which generates reference voltages of ±10V from the ±15V supply voltages.

4.5.1 Control Logic Registers

The control logic register circuit consists of address decoder U1 and data registers U2-U6. The address decoder is enabled by a logic low on the $\overline{\text{ANA2}}$ line (J16 pin 12). The decoder provides a logic low on one of its five output lines; the output line selected is determined by the binary value of the three input address lines. For example, an address of "000" selects output Y0, while an address of "100" selects output Y4. The outputs are used to latch data into the data registers.

The five data registers are octal type "D" flip-flops that latch data from the buffered data bus (J16 pins 1 through 8) onto the register output pins, where it is continuously available to the remainder of the circuits on the board. Each register is clocked by the microprocessor and address decoder at a time when the data on the buffered data bus is valid for that particular register. Clocking occurs on the rising edge of the clock pulse, at the end of the momentary low on the clock line.

4.5.2 Burst Counter

The burst counter enables the function generator for a predetermined number of cycles when the burst mode is selected and the circuit is manually or externally triggered. The two circuit groups within the burst counter are the burst logic and the preset counter. Figure 4-21 shows a simplified functional block diagram of the burst counter circuit.

The preset counter counts the number of waveform cycles that occur during the burst. When the predetermined number of cycles have been counted, the counter circuit signals the burst logic via a logic low on the "$\overline{\text{end-of-count}}$" line.

The burst logic, when triggered in the burst mode, gates the SQS square wave output of the function generator through to the counter circuit and latches the burst counter output line (TRGI) high for the duration of the count. If the burst mode is not selected, the burst logic gates the trigger or gate input (TRGO) directly through to the output line (TRGI). The TRGI line is routed to the

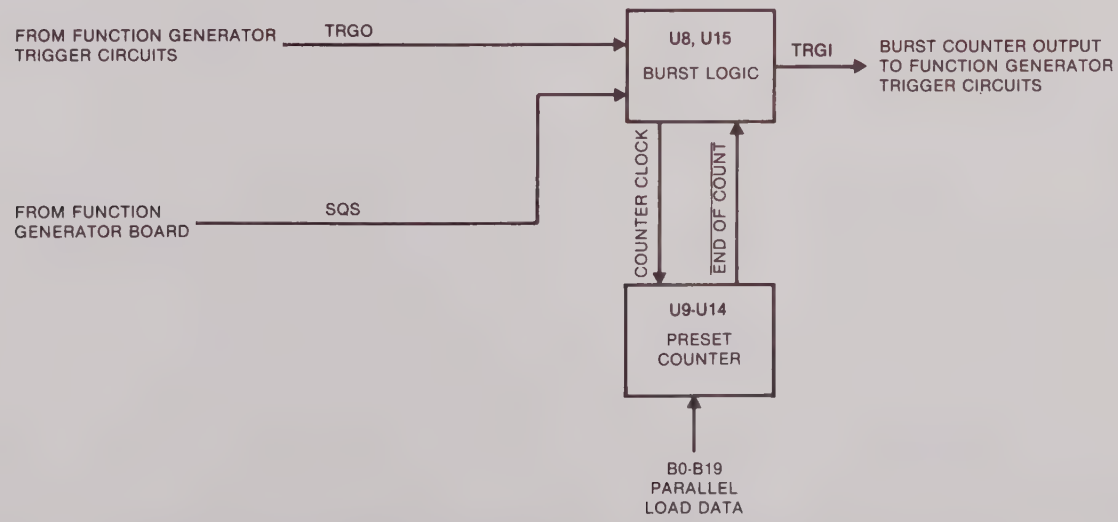


Figure 4-21. Simplified Functional Block Diagram, Burst Counter Circuit

remainder of the trigger logic on the function generator board via J15 pin 7.

The preset counter is composed of presettable 4-bit binary counters U9 through U13, and terminal count detector NAND gate U14. When the preset counter receives clock pulses from the burst logic, it preloads data from the data registers then counts pulses from the burst clock select gates, counting upwards from the preloaded value. When the final count value is reached, the circuit commands the burst logic to return the TRGI output line low.

Although U9 through U13 are capable of counting to 1,048,575 ($2^{20}-1$), the maximum count is limited to 1,048,200 by terminal count detector U14. The binary equivalent of 1,048,200 is $2^3 + 2^7 + 2^9 + \ldots + 2^{19}$, and only those counter output lines are monitored by U14. (Note that some of the counter outputs are not used.) The binary number that will be loaded from the data registers into the preset counter is this maximum count minus the desired count plus one. (The burst logic will always allow one extra cycle after the preset counter reaches maximum count.)

At maximum count, all of the U14 inputs are high, and the output is low. This logic low is applied to the counter $\overline{\text{LOAD}}$ inputs, and also to the burst logic.

The burst logic consists of NAND gates U8C through U8A, and type "D" flip-flops U15A and U15B. This circuit is activated by a trigger pulse (TRGO) from the trigger circuits on the function generator board, and provides a logic high on the TRGI line. In the burst mode, the TRGI line is held high for the duration of the burst. When the burst mode is not selected, the TRGI output pulse is a copy of the input pulse at TRGO. The TRGI output is applied to the function generator (via J16 pin 7).

In the burst mode, the BURST line is at a logic high, and the $\overline{\text{BURST}}$ line is at a logic low. The logic low on the $\overline{\text{BURST}}$ line disables NAND gate U8A and enables NAND gate U8B via the constant high at the U8A output. The logic low on the $\overline{\text{BURST}}$ line is also applied to the data input of flip-flop U15A.

Initially, the counter is in the maximum-count condition, and the output of the terminal count detector is at a logic low. This logic low is applied to the $\overline{\text{LOAD}}$ inputs of counter stages U9 through U13 to enable loading of the preset data at the next clock pulse. The same logic low disables NAND gate U8C to prevent the SQS output of the function generator from clocking the counter, and enables NAND gate U8D (via the logic high on the U8C output) to allow the load pulse from U15A to clock the preset data into the counter stages.

A positive logic transition at the TRGO trigger input clocks the U15A Q output low. The negative-going transition at the U15A Q output is inverted by U8D and applied to the counter clock inputs to load the preset data. As soon as the counter is loaded with preset data, it is no longer at the maximum count condition and the U14 output goes high, disabling the counter $\overline{\text{LOAD}}$ inputs and enabling NAND gate U8C. However, at this point, the SQS square wave input cannot yet reach the counter clock inputs because NAND gate U8D is disabled by a logic low from U15A.

After a time delay determined by R10 and C13, the logic low at the U15A Q output is applied to the U15B $\overline{\text{SET}}$ input to set the U15B $\overline{\text{Q}}$ output low. This low is inverted by U8B and provides a logic high on the TRGI output line. The logic low at the U15B $\overline{\text{Q}}$ output is also applied back to the direct $\overline{\text{SET}}$ input of U15A to set the U15A Q output high. The logic high from the U15A Q output enables NAND gate U8D to pass the SQS clock pulses to the counter.

When the counter reaches maximum count, the output of the terminal count detector U14 goes low, disabling NAND gate U8C and preventing clock pulses from reaching the counter. U14 also supplies a logic low to the data input of flip-flop U15B. The next positive transition of the SQS line will clock the U15B $\overline{\text{Q}}$ output high, causing U8B to return the TRGI output line to a logic low state.

When the burst mode is not selected, the BURST line is at a logic low state and the $\overline{\text{BURST}}$ line is at a logic high. The logic low on the BURST line holds the $\overline{\text{CLEAR}}$ input of flip-flop U15B low, maintaining a logic high from the U15B $\overline{\text{Q}}$ output to enable NAND gate U8B. The logic high on the $\overline{\text{BURST}}$ line enables NAND gate U8A. Any trigger signal applied to the TRGOB line will be gated through U8A and U8B to the TRGI output.

Resistors R84 and R85, marked "TRIM" on the schematic, are external pull-up resistors to increase speed and reduce power consumption of the preset counter. These resistors are not required for type 74LS counters, but space has been provided for them on the board for future use with type 74HC devices. These resistors, when used, have a typical value of 10kΩ.

4.5.3 ±10 Volt Reference

The ±10 volt reference circuit generates reference voltages of ±10V from the ±15V supply voltages.

U7B amplifies the 6.2V drop across zener diode CR1 to provide the +10V reference. Unity gain inverting amplifier U7A inverts the +10V output of U7B to create the −10V reference.

4.5.4 Pulse Generator

The pulse generator consists of two major circuit groups; the delay one-shot and the width one-shot. The delay one-shot is triggered by the SQS square wave output of the function generator, and after the programmed delay interval triggers the width one-shot via a pulse on the DELTOWID line. The width one-shot starts timing when triggered by the delay one-shot, and forces its output line high for the programmed duration of the pulse. The output of the width one-shot is routed to the function generator board via the PLSI line.

Both the delay one-shot and the width one-shot perform the timing function by comparing the instantaneous voltage of a linear ramp to an adjustable dc threshold voltage. Triggering the one-shot at the start of the timing interval enables the ramp circuit and causes the ramp voltage to start rising. The timing interval ends when the instantaneous voltage of the ramp becomes equal to the adjustable threshold voltage at the other input of the comparator.

The delay and the width one-shot circuits are almost identical, with the exception that the delay circuit also contains the double pulse logic.

4.5.4.1 Delay One-shot

Overall operation of the delay one-shot will be discussed before the individual circuits are explained.

The delay DAC circuit produces a voltage that is proportional (within the selected range) to the programmed pulse delay. The amplitude and offset of the DAC circuit output voltage are modified by the delay range calibration circuit, and the resulting threshold voltage is applied to the comparator logic.

The comparator logic circuit is enabled by a high on the DELON line, and triggered by the rising edge of the SQS square wave from the function generator. As soon as the comparator logic circuit is triggered, it enables the ramp circuits. When the rising ramp voltage becomes equal to the comparator threshold voltage, the comparator logic circuit resets the ramp and (via the double pulse logic) pulses the DELTOWID line high.

The DELTOWID line may also be pulsed high by the undelayed SQS square wave if the $\overline{\text{DELPLS}}$ control line is high.

Delay ranges are changed by selecting various combinations of ramp capacitor and charging current. As previously mentioned, delay within the selected range is controlled by the amplitude of the comparator threshold voltage.

The delay one-shot contains the following individual circuits:

1. The three-decade current source, which generates a constant current of either 2 ma, 0.2 ma or 0.02 ma for charging the selected ramp capacitor.
2. The range capacitors circuit, which selects a ramp capacitor of either 100 pF (including stray capacitance), 0.01 μF or 1 μF.
3. The ramp reset circuit, which is driven by the comparator logic to either hold the ramp capacitor in a discharged condition, enable the ramp capacitor to charge, or rapidly discharge the ramp capacitor.
4. The FET buffer, a high-impedance input unity gain buffer amplifier that prevents the load presented by the comparator logic circuit from affecting the charge rate of the ramp capacitor.
5. The delay DAC circuit, which generates a threshold voltage proportional to the value (within the selected range) of the programmed pulse delay.
6. The delay range calibration circuit, which modifies the value of the delay DAC output voltage to allow calibration on the individual delay ranges.
7. The comparator logic, which compares the instantaneous ramp voltage to the threshold voltage output of the delay range calibration circuit. The comparator logic drives both the ramp reset circuit and (via the double pulse logic) the width one-shot circuit.
8. The double pulse logic, which selects either an undelayed pulse, a delayed pulse, or both (a double pulse).

4.5.4.1.1 Three Decade Current Source

The three-decade current source generates a constant current of either 2 ma, 0.2 ma or 0.02 ma for charging the selected ramp capacitor. It generates the constant current by holding a constant voltage across the selected range resistor.

A logic low on one of delay range control lines ($\overline{\text{DR4}}$-$\overline{\text{DR6}}$) turns on one of the three solid-state switches (U20A-U20C), connecting one of the range resistors (R33-R35) between the +15V supply and the source of FET Q1.

U24A compares the voltage at the Q1 source to a fixed level of +10V from voltage divider R31/R32, and drives Q1 to whatever conduction level is required to hold the Q1 source at the same +10V level. The result is a constant 5V drop across the selected range resistor, the therefore a constant current through the resistor. This resistor current also flows through FET Q1 and buffer Q2, then charges the selected range capacitor when the ramp is enabled. Charging the capacitor from a constant-current source results in a linear increase of voltage

across the capacitor, instead of the exponential increase that would occur if only a series resistance were used.

4.5.4.1.2 Range Capacitors Circuit

The range capacitors circuit selects one of three capacitors as the ramp capacitor to be charged by the three-decade current source. Various combinations of three available values of charging current and three different values of ramp capacitor are used to create the seven pulse delay ranges in the Wavetek 271.

The range capacitors circuit consists of capacitors C34 to C36, relays K1 and K2, and relay drivers Q4 and Q5. A logic high on both $\overline{DR1}$ and $\overline{DR7}$ leaves both relays de-energized, selecting a ramp capacitor value of 100 pF (the parallel value of C34 and stray circuit capacitance). A logic low on control line $\overline{DR1}$ or $\overline{DR7}$ turns on relay driver Q4 or Q5, energizing relay K1 or K2 to select capacitor C35 (0.01 μF) or C36 (1 μF). Table 4-2, Pulse Delay Ranges, shows the logic state of the delay control lines ($\overline{DR0}$ through $\overline{DR7}$) for the various delay ranges. (These ranges are the values programmed by the operator, and include the fixed 40 ns delay of the entire instrument.) Note that control lines $\overline{DR0}$, $\overline{DR2}$ and $\overline{DR3}$ are not used for the selection of current source and ramp capacitor; these lines are used only by the delay range calibration circuit.

Table 4-2. Pulse Delay Ranges

Delay Range	Control Line Logic States							
	$\overline{DR0}$	$\overline{DR1}$	$\overline{DR2}$	$\overline{DR3}$	$\overline{DR4}$	$\overline{DR5}$	$\overline{DR6}$	$\overline{DR7}$
80 ns-139 ns	L	H	H	L	H	H	L	H
140 ns-1.03 μs	L	H	L	H	H	L	H	H
1.04 μs-9.99 μs	L	H	H	H	L	H	H	H
10 μs-99.9 μs	H	L	H	H	H	L	H	H
100 μs-999 μs	H	L	H	H	L	H	H	H
1 ms-9.99 ms	H	L	H	H	H	L	H	L
10 ms-99.9 ms	H	L	H	H	L	H	H	L

4.5.4.1.3 Ramp Reset Circuit

The ramp reset circuit holds the ramp capacitor discharged before the timing interval begins, allows it to charge during the timing interval, and rapidly discharges the capacitor at the end of the timing interval. The input to the circuit is the constant current from the three-decade current source. The output of the circuit is the line to the ramp capacitor. The three control lines to the circuit from the comparator logic circuit are RAMP ENABLE, RAMP HOLD and $\overline{FAST\ RESET}$ lines. Figure 4-22 shows the logic states for these three lines at each stage of the ramp waveform. Figures 4-23a through 4-23c are simplified schematic diagrams of the ramp reset circuit that illustrate circuit operation during ramp capacitor charge, discharge and hold.

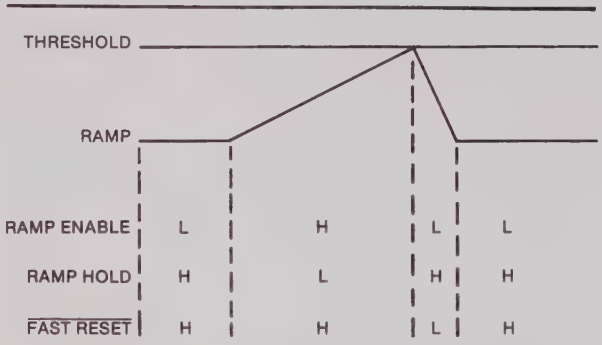


Figure 4-22. Logic States for Ramp Reset Circuit Control Lines

A. Before the timing interval starts:

1. The RAMP ENABLE line is low and the cathode of CR5 is approximately one junction drop below ground potential. CR4 is forward biased to provide a path for the constant current (I) from the current source through CR4 and R36 to the −15V supply. The junction of CR4 and CR3 is approximately at ground potential; therefore no current will flow through CR3 into the ramp capacitor.
2. The RAMP HOLD line is high, and current flows from this line through CR11 to ground and through CR10 to the −15V supply. Since the anodes of the two diodes are connected together and the cathode of CR11 is grounded, the cathode of CR10 (and the gate of FET Q3) will also be at ground potential. Without any reverse bias on its gate, Q3 will conduct and will hold the ramp capacitor discharged.
3. The $\overline{FAST\ RESET}$ line is high. CR7 is reverse biased, preventing the ramp capacitor from discharging through R37 to the −15V supply.

B. As soon as the timing interval starts:

1. The RAMP ENABLE line goes high, reverse biasing CR4 to turn off the circuit path from the current source to the −15V supply.
2. The RAMP HOLD line goes low. Resistors R38 and R39 form a voltage divider that applies a reverse bias of several volts to the gate of Q3,

turning the FET off and removing the capacitor discharge path to ground.

3. The $\overline{\text{FAST RESET}}$ line remains high, reverse biasing CR7 to prevent the ramp capacitor from attempting to discharge to the −15V supply.

C. At the end of the timing interval:

1. The RAMP ENABLE line is set low, to forward bias CR4 and provide a path from the current source to the −15V supply.
2. The RAMP HOLD line is set high to remove the reverse gate bias on Q3, allowing it to conduct to provide a discharge path to ground to hold the ramp capacitor discharged.
3. The $\overline{\text{FAST RESET}}$ line is set low to forward bias CR7 and provide a discharge path from the ramp capacitor to the −15V supply. (This discharge path is faster than the path to ground through the resistance of the Q3 FET.)

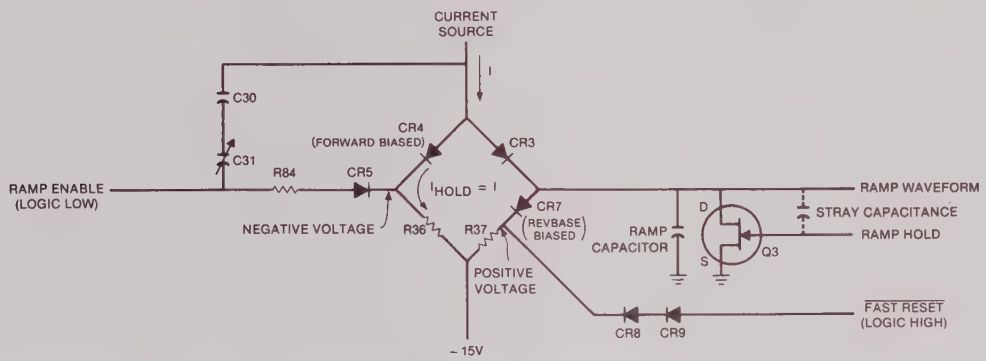


Figure 4-23a. Simplified Schematic Diagram Ramp Reset Circuit (Hold Condition)

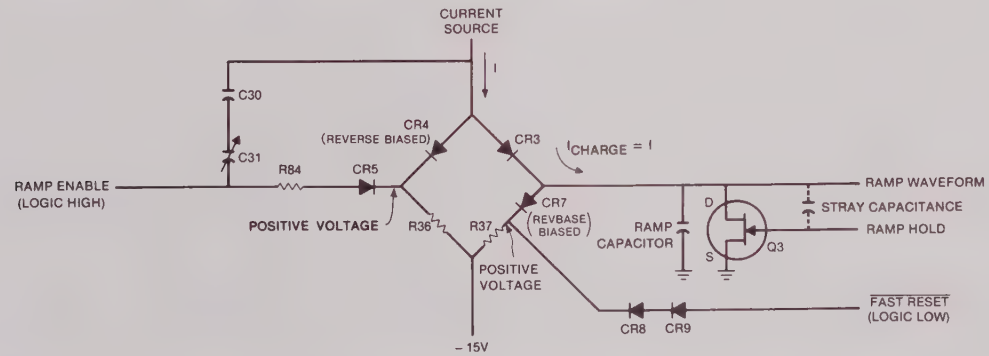


Figure 4-23b. Simplified Schematic Diagram Ramp Reset Circuit (Capacitor Charging)

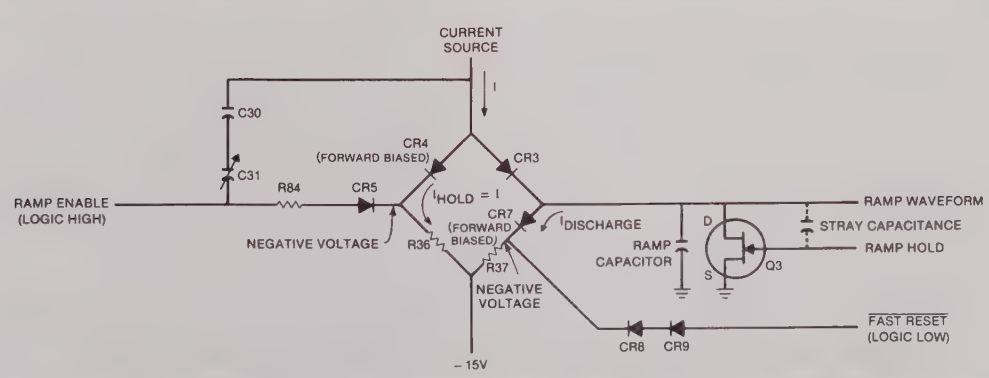


Figure 4-23c. Simplified Schematic Diagram Ramp Reset Circuit (Capacitor Discharging)

D. After the ramp capacitor is discharged:

1. The RAMP ENABLE line remains low to provide a path from the current source to the −15V supply.
2. The RAMP HOLD line remains high to bias on Q3, allowing it to hold the ramp capacitor discharged.
3. The $\overline{\text{FAST RESET}}$ line is returned high to prevent the ramp capacitor from attempting to charge to a negative voltage from the −15V supply.

Capacitors C30 and C31 cancel the effect of the stray capacitance between the gate and drain terminals of Q3.

When the RAMP HOLD line is set low at the beginning of the timing interval, capacitive coupling through the stray gate to drain capacitance of Q3 attempts to pull the voltage on the ramp capacitor slightly below ground level. If left uncorrected, this would slightly increase the time required for the ramp capacitor to charge to the comparator threshold voltage. An equal and opposite charge is coupled from the positive-going RAMP ENABLE line through C30 and C31. Since the RAMP HOLD and RAMP ENABLE lines are driven from the complementary outputs of the same flip-flop (U22A in the comparator logic), their transitions will always be in opposite directions and always at the same time.

4.5.4.1.4 FET Buffer Circuit

The FET buffer circuit is a high input impedance unity gain amplifier that prevents the load of the comparator logic from affecting the charge time of the ramp capacitor. The circuit consists of FET Q6, transistors Q7 and Q8 and operational amplifier U24B.

Q6 and Q7 are connected in a "totem-pole" configuration to drive the Q8 base circuit. Q6 is a source-follower that is driven by the ramp voltage to provide pull-up to the Q8 base; Q7 provides pull-down to the -15V supply. The Q8 output stage is an emitter-follower.

Operational amplifier U24B cancels any non-linearities caused by Q6-Q8. The two inputs of U24B are driven by the unbuffered and buffered ramps. Any error caused by a difference in instantaneous voltages on the two ramps is amplified and applied to the emitter of Q7 to force the Q8 output voltage to be exactly equal to the Q6 gate input voltage. For example, if the buffered ramp voltage is less than the input ramp voltage, the U24B output goes positive. This positive voltage is applied through R43 to the emitter of Q7, reducing the collector current in Q7 and allowing Q6 to pull the Q8 base higher. Conversely, if the buffered ramp voltage is greater that the input ramp voltage, the U24B output swings negative to increase the Q7 collector current and provide more pull-down for the Q8 base.

4.5.4.1.5 Delay DAC Circuit

The delay DAC circuit generates a negative voltage proportional to the value (within the selected range) of the programmed pulse delay. The circuit consists of Digital-to-Analog Converter U16 and current-to-voltage converter U17A.

Digital-to-Analog Converter U16 generates an output current that is proportional to both the input reference voltage and the numerical value of the data latched from the main data bus. Full-scale output current is equal to 1023/1024 times the input reference current. The input reference current is equal to the input reference voltage divided by R, where R is the resistance value used in the internal R/2R ladder network (R≅15kΩ). The exact value of R is not important; the DAC contains an internal feedback resistor (pins 12 and 14) for the U17A current-to-voltage converter, and as long as this resistor is matched to the ladder network resistors, any errors caused by resistance variation will cancel at the output of U17A.

U16 has two complimentary current outputs; I_{out} and $\overline{I_{out}}$. The $\overline{I_{out}}$ current is equal to the full scale output current minus the I_{out} current. The $\overline{I_{out}}$ output is grounded, and not used.

U16 contains internal registers to latch 10 bits of data from the 8 bit data bus. Data is latched from the bus when the $\overline{\text{ANA3}}$ control line pulls the DAC $\overline{\text{WR}}$ and $\overline{\text{XFER}}$ control inputs (pins 2 and 4) low. The BADR0 control line, connected to the DAC BYTE1/$\overline{\text{BYTE2}}$ control input (pin 3), determines whether the data on the bus will will be latched into the 8-bit register or the 2-bit register. Data bus lines BDATA6 and BDATA7 are wired to the DAC inputs for bits D6 and D7, and also the inputs for bits D8 and D9. When the BADR0 line is high, data is written into the 8-bit latch. When the BADR0 line is low, a write operation latches the new data (DAC bits D8 and D9) on lines BDATA6 and BDATA7 into the 2-bit register.

Latching of data into DAC U16 is enabled by a low on the BADR2 line, which is connected to the U16 $\overline{\text{CHIP SELECT}}$ input.

U17A is an operational amplifier used as a current-to-voltage converter. The circuit is configured as an inverting amplifier, using the resistor internal to the DAC (pins 12 and 14) as the feedback resistor. The operational amplifier will drive its output to whatever voltage is required to keep its two input pins at the same level. Since the non-inverting input (pin 3) of U17A is grounded, the inverting input (pin 2) becomes a "virtual ground", and the current in the feedback resistor is equal to the DAC output current. The U17A output voltage is then equal to the DAC output current times the value of the feedback resistor. Full-scale output voltage is equal to 1023/1024 times the U16 input reference voltage. As

previously mentioned, the exact value of the internal feedback resistor is not important, as long as it is matched in value to the resistors in the DAC R/2R ladder network.

4.5.4.1.6 Delay Range Calibration Circuit

The delay range calibration circuit allows calibration of pulse delay on the individual delay ranges by modifying the amplitude and offset of the comparator threshold voltage. The circuit consists of inverting operational amplifier U17D, solid-state switches U18A, U18D, U19A and U19D, and associated resistors and potentiometers.

Control lines $\overline{DR0}$ and $\overline{DR1}$ control solid-state switches U18A and U18D, which switch potentiometers R14 and R15 into or out of the circuit to allow gain adjustment on the individual delay ranges. As shown in table 4-2, a logic low on line $\overline{DR0}$ switches in R14 on the lowest three ranges, while a low on $\overline{DR1}$ inserts R15 into the circuit on the four highest ranges.

Switches U19D and U19A are controlled by lines $\overline{DR2}$ and $\overline{DR3}$, and operate in conjunction with potentiometer R13 to control the amount of offset voltage applied to the amplifier. $\overline{DR3}$ switches in R17 on the lowest delay range, while $\overline{DR2}$ switches in R16 on the next highest range. This offset is necessary to compensate for comparator logic switching delays.

A fixed amount of offset voltage is applied to the amplifier from potentiometer R21 via resistive voltage divider R19/R20. This offset voltage is constant, regardless of delay range selected.

Table 4-2 lists the state of each delay range control line for the various delay ranges.

4.5.4.1.7 Comparator Logic Circuit

The comparator logic circuit compares the instantaneous ramp voltage to the threshold voltage output of the delay range calibration circuit. The comparator logic drives both the ramp reset circuit and (via the double pulse logic) the width one-shot circuit.

The circuit consists of comparators U21A and U21B, and type "D" flip-flops U22A and U22B. U21A and U22A perform the timing function by comparing the instantaneous ramp voltage to the threshold voltage. U21B and U22B monitor the ramp voltage during discharge of the ramp capacitor, and remove the drive on the $\overline{FAST\ RESET}$ line at the end of the discharge period.

The comparator logic circuit is initially enabled by a high on the DELON line and triggered by the rising edge of the SQS square wave from the function generator board. The high on the DELON line is applied to the data input of flip-flop U22A, and the SQS square wave clocks the high at the U22A data input through to the output. This sets the RAMP ENABLE line (Q output) high and the RAMP HOLD line ($\overline{Q}$ output) low, and the ramp capacitor starts charging.

As soon as the ramp voltage at the U21A inverting input (pin 2) exceeds the threshold at the non-inverting input (pin 1), the comparator output goes low. This logic low resets U22A to cause a low on the RAMP ENABLE line and a high on the RAMP HOLD line. The U21A comparator output also sets flip-flop U22B, causing a low on the $\overline{FAST\ RESET}$ line (U22B-$\overline{Q}$). As soon as the ramp capacitor discharges below the U21A threshold voltage, the U21A comparator output returns to a logic high state, removing the low at the U22B $\overline{SET}$ input.

Comparator U21B compares the ramp voltage to a fixed threshold voltage, and removes the low on the $\overline{FAST\ RESET}$ line when the ramp capacitor is discharged. (This prevents the ramp capacitor from being discharged to less than ground level.) The U21B threshold is usually zero volts, but on the three lowest ranges a low on line $\overline{DR0}$ closes solid-state switch U20D, generating a small (0.7V) threshold voltage from voltage divider R25/R26. This causes the comparator to change states slightly before the ramp capacitor is fully discharged to compensate for switching delays in the circuit.

4.5.4.1.8 Double Pulse Logic

The double pulse logic selects either an undelayed pulse, a delayed pulse, or both (a double pulse). The circuit consists of NAND gates U23A and U23D, voltage divider R29/R30, and coupling capacitor C26.

The two inputs of NAND gate U23A are connected to the $\overline{DELPLS}$ line and the SQS output of the function generator. A logic high on the $\overline{DELPLS}$ line allows the SQS square wave to be gated through to the U23A output. The U23A output is capacitively coupled to the midpoint of voltage divider R29/R30.

Voltage divider R29/R30 holds the U23D pin 12 input just above the dividing line between TTL logic low and TTL logic high. If U23A is enabled by a logic high on the $\overline{DELPLS}$ line, the negative-going transitions of the inverted SQS square wave at the output of U23A are capacitively coupled through C26, and momentarily drive the output of voltage divider R29/R30 to a logic low.

NAND gate U23D is driven by voltage divider R29/R30, and also by the output of comparator U21A. A logic low on either input line will cause a logic high on the DELTOWID (delay-to-width) output line.

An undelayed pulse on the DELTOWID line is produced if the $\overline{DELPLS}$ control line is high. A delayed pulse is produced if the DELON line is high. A double pulse results if both lines are high.

4.5.4.2 Width One-shot

The width one-shot circuit is identical to the delay one-shot with the following exceptions:

1. The width one-shot is triggered by a positive-going transition on the DELTOWID line from the delay one-shot circuit.
2. The output of the width one-shot is routed to the pulse input of the function generator board via the PLSI line.
3. The width DAC $\overline{\text{CHIP SELECT}}$ input is driven by the BADR1 control line.
4. R63 is a test-select resistor with a nominal value of 619Ω.
5. Because external circuit delays affect pulse delay but not pulse width, the limits of the faster delay and width ranges differ by 40 ns. This 40 ns difference becomes insignificant on the higher ranges because of parameter rounding to three significant digits by the microprocessor.

Table 4-3, Pulse Width Ranges, shows the logic state of the width control lines ($\overline{\text{WR0}}$ through $\overline{\text{WR7}}$) for the various width ranges.

Table 4-3. Pulse Width Ranges

Width Range	Control Line Logic States							
	$\overline{\text{WR0}}$	$\overline{\text{WR1}}$	$\overline{\text{WR2}}$	$\overline{\text{WR3}}$	$\overline{\text{WR4}}$	$\overline{\text{WR5}}$	$\overline{\text{WR6}}$	$\overline{\text{WR7}}$
40 ns-99.9 ns	L	H	H	L	H	H	L	H
100 ns-999 ns	L	H	L	H	H	L	H	H
1 µs-9.99 µs	L	H	H	H	L	H	H	H
10 µs-99.9 µs	H	L	H	H	H	L	H	H
100 µs-999 µs	H	L	H	H	L	H	H	H
1 ms-9.99 ms	H	L	H	H	H	L	H	L
10 ms-99.9 ms	H	L	H	H	L	H	H	L

4.5.5 Power Distribution

The +15V, −15V and +5V dc power for all circuits enters the board at the J17 AUXILIARY POWER CONNECTOR. The lines are filtered by capacitors C15-C17. Additional filtering is provided by small value bypass capacitors at various locations on the board.

4.6 MODEL DIFFERENCES

Wavetek Model 271 Function Generators with serial numbers less than 7230039 have several minor differences in the Microprocessor/Power Supply Board. Section 7 contains a schematic diagram (drawing number 0103-00-0919) of the earlier board revision. On the earlier version of the Model 271 Microprocessor/Power Supply Board:

1. $\overline{\text{MASTER RESET}}$ capacitor C1 was 100 µF, 16V. The $\overline{\text{MASTER RESET}}$ function ($\overline{\text{MR}}$) was performed entirely by charging this capacitor through R8; operational amplifier U27 was not used in the $\overline{\text{MASTER RESET}}$ circuit.
2. Operational amplifier U27A was used in the battery test circuit as a voltage follower amplifier providing an output equal to the comparator reference voltage. It was used to convert the ± 15V output of the U27B comparator to TTL logic levels by summing the two voltages through R30 and R31.
3. The second RAM (U12) and memory backup battery BT1 were optional (Option 001).
4. There was no RAM PWR connection to auxiliary connector J4-19.
5. Alternate bus driver U8A pin 11, the DIRECTION CONTROL line (DC), was connected to +5V.
6. IEEE 488 Bus Driver U8B pin 1, the SEND/$\overline{\text{RECEIVE}}$ line (S/$\overline{\text{R}}$), was connected to +5V.
7. The $\overline{\text{CHIP ENABLE}}$ ($\overline{\text{CE}}$) input of U9 (pin 20) was connected to the ROM1 line.
8. The $\overline{\text{CHIP ENABLE}}$ ($\overline{\text{CE}}$) input of U10 (pin 20) was connected to the ROM2 line.
9. The $\overline{\text{ANA2}}$ and $\overline{\text{ANA3}}$ lines were buffered by auxiliary buffer U28 (pins 4, 6, 16 and 14) and appeared at the auxiliary connector J4 (pins 12 and 13) as $\overline{\text{BANA2}}$ and $\overline{\text{BANA3}}$.
10. Ground test points TP3, TP4 and TP5 were not present on the earlier revision board.
11. If applied power is interrupted and immediately reapplied, the instrument circuits may "hang up". A 3 second wait before reapplying power ensures normal instrument operation.

SECTION 5
CALIBRATION

5.1 FACTORY REPAIR

Wavetek maintains a Customer Service department. If an instrument is returned to Wavetek for repair or calibration, a detailed description of the specific problem should be attached to minimize turn around time.

5.2 CALIBRATION

NOTE

The completion of these calibration procedures returns the instrument to correct calibration. All limits and tolerances given in these procedures are calibration guides and should not be interpreted as instrument specifications. Instrument specifications are given in section 1 of this manual.

Table 5-1 lists the equipment required to perform the calibration procedures in table 5-2.

The setup for each calibration step and a displayed operator cue are contained within the firmware. Calibration steps and cues can be accessed by pressing RCL 1001 EXEC, RCL 1002 EXEC, etc. for each step of the calibration procedure in table 5-2. Calibration points are shown in figures 5-1 through 5-3.

Periodic calibration is needed because of component aging, which depends on instrument on-time and environment. Use six months as an initial calibration period. If possible keep records of the parameter values and modify the time between calibration if the records indicate.

Before beginning the calibration procedure, verify the correct placement of the following jumpers located on the function generator board (ref: figure 5-2):

VCG Jumper	E9 to E10
Trig In Jumper	E13 to E14

To gain access to the Microprocessor/Power Supply board (steps 1 to 3), remove the bottom cover (2 screws).

To gain access to the Function Generator (steps 4 to 28) and pulse boards (steps 29 to 38), remove the top cover (2 screws), next remove the two screws on the right of the pulse board, and lift the pulse board up to access Function Generator board adjustments (the pulse board pivots on the left side).

NOTE

1. *EXEC (Execute), required to implement parameter value change, has been omitted from the calibration procedure.*
2. *Each step (RCL 1001, 1002 etc) also can be increented and executed by using the cursor control (ref: paragraph 3.4.5.8).*
3. *When using the Function Output BNC, it must be terminated with a 50Ω termination.*

Table 5-1. Calibration Test Equipment

Instrument	Suggested Model	Comment
Digital Voltmeter	Fluke 8050A	DC accuracy: 0.01% AC accuracy (true rms): 0.2%
Distortion Analyzer	N/A	Frequency range: 5 Hz to 100 kHz Distortion measurement: 0.1 to 100%
Frequency Counter	HP5334A	Frequency range: 0.5 Hz to 13 MHz Frequency accuracy: ±1 ppm

Table 5-1. Calibration Test Equipment (Continued)

Instrument	Suggested Model	Comment
Oscilloscope		
Main frame	Tektronix 7904	Bandwidth: dc to 500 MHz
Plug-in Vertical Amplifier	Tektronix 7A26	Bandwidth: dc to 200 MHz Sensitivity: 5 mV to 5V/div Input impedance: 1 MΩ
Dual Time Base	Tektronix 7B53A	Time/div: 5 ns to 5 s
Sampler	Tektronix 7S14	Bandwidth: dc to 1 GHz
Terminations	Tektronix 011-0129-00 Tektronix 011-0049-01	50Ω ± 0.1%, 2W 50Ω ± 2.0%, 2W
Attenuator	Tektronix 011-0059-02	10X, 50Ω, 2W
Coax Cable	Tektronix 012-0057-01	50Ω, 3 ft length

Amplitude and Offset calibration requires a 50 ± 0.05Ω termination. If a precision termination is not available, a correction factor (K) can be derived, which can be used to calculate a normalized calibration value.

K is derived as follows:

$$K = \frac{R + 50}{2R}$$, where R is the value of the terminator used.

To calulate a normalized calibration value, divide the value from Desired Results by K. Or, multiply the measurement by K, which should equal the value from Desired Results.

Table 5-2. Calibration Procedure

NOTE: Open column indicates previous entry remains applicable

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
NOTE: Steps 1 through 3 are power supply adjustments (see figure 5-1).							
1	+15V SUPP, R39	DVM (dc mode)	J3-1, TP2 (GND)	RCL 1001	R39	+15 ± .002 Vdc	
2	−15V SUPP, R47		J3-5, TP2 (GND)	RCL 1002	R47	−15 ± .002 Vdc	
3	−10.24V REF, R16		TP1, TP2 (GND)	RCL 1003	R16	−10.24 ± .002 Vdc	
NOTE: Steps 4 through 28 are function generator adjustments (see figure 5-2)							
4	NODE BAL, R99	DVM (dc mode)	J23-9, TP1 (GND)	RCL 1004	R99	0 ± 1.0 Vdc	
5	TRI BALANCE, R60		J23-7, TP1 (GND)	RCL 1005	R60	0 ± .002 Vdc	
6	VCG ZERO, R11		VCG IN BNC (Front Panel)	RCL 1006	R11	0 ± .001 Vdc	

Table 5-2. Calibration Procedure (Continued)

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
7	HI SYMM, R23	Oscilloscope	FUNC OUT (terminate with 50Ω)	RCL 1007	R23	50% Duty Cycle ±0.5 μs	
8	LO SYMM, R15			RCL 1008	R15	50% Duty Cycle ±0.5 μs	
9	LO FREQ, R12	Frequency Counter	FUNC OUT (terminate with 50Ω)	RCL 1009	R12	10 ± .1 Hz	
10	HI FREQ, R8			RCL 1010	R8	999 ±1.0 Hz	Steps 9 and 10 interact; repeat if necessary.
11	1 MHz, C43			RCL 1011	C43	1 ± .001 MHz	After making the initial adjustments in steps 11 and 12, record the frequency in each step. Place the sweep board in the operating position. Record the new frequency for each step. Note the difference in frequency. Lift up the sweep board. Increase the frequency by the frequency difference. Repeat steps 11 and 12 if necessary.
12	9.99 MHz, R45			RCL 1012	R45	9.99 ± .01 MHz	
13	100 kHz, C45	Frequency Counter	FUNC OUT (terminate with 50Ω)	RCL 1013	C45	100 ± .1 kHz	
14	999 kHz, R46			RCL 1014	R46	999 ± 1 kHz	Steps 13 and 14 interact; repeat if necessary.
15	10 Hz SYM, R117	Oscilloscope		RCL 1015	R117	Symmetry 50% ± .1%	
16	0.999 Hz, R105	Frequency Counter		RCL 1016	R105	.999 ± .001 Hz	
17	99.9 Hz, R112			RCL 1017	R112	99.9 ± .1 Hz	
18	SINE DIST	Distortion Analyzer	FUNC OUT (terminate with 50Ω)	RCL 1018	R142 R154 R157 R255	<.3%	Adjust for minimum distortion.
19	MULT BAL, R241	Oscilloscope		RCL 1019	R241	⩽.070 Vp-p	Adjust for minimum amplitude variation. Steps 18 and 19 interact; repeat if necessary.
20	OFFSET 0, R237	DVM (dc mode)	FUNC OUT (terminate with	RCL 1020	R237	0 ± .005 Vdc	
21	OFFSET +5, R208		.1% 50Ω load)	RCL 1021	R208	5 ± .005 Vdc	
22	HI AMPL, R242	DVM (ac mode)		RCL 1022	R242	3.536 ± .01 Vac	
23	LO AMPL, R251			RCL 1023	R251	.357 ± .002 Vac	
24	TRI AMPL, R148			RCL 1024	R148	2.887 ± .003 Vac	
25	SQR LOWER, R168	DVM (dc mode)		RCL 1025	R168	−5 ± .005 Vdc	

Table 5-2. Calibration Procedure (Continued)

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
26	SQR UPPER, R164	DVM (dc mode)	FUNC OUT (terminate with .1% 50Ω load)	RCL 1026	R164	5 ± .005 Vdc	
27	ATTEN ADJ, R295			RCL 1027	R295	.500 ± .001 Vdc	
28	WAVEFORM C97, C122, R96	Oscilloscope with Sampler Plug in	FUNC OUT (terminate with X10, 50Ω attenuator)	RCL 1028	C97 C122 R96	Aberrations ≤3.3% ± 50 mV Rise/Fall <14.5 ns	Move VCG jumper to E10 and E11.
	NOTE: Steps 29 to 38 are pulse adjustments (See figure 5-3).						
29	9.99 ms WIDTH R52	COUNTER set to make width measurement	FUNC OUT terminate with 50 ohms	RCL 1029	R52	9.99 ms ± .01 ms	CAL points and adjustments for steps 29 to 38 refer to pulse board with board in position
30	1 ms WIDTH R58			RCL 1030	R58	1.00ms ± .001ms	Repeat steps 29 and 30 as necessary.
31	9.99 μs WIDTH			RCL 1031	R51	9.99μs ± .01μs	
32	1 μs WIDTH C52			RCL 1032	C52	1.00μs ± .001μs	Repeat steps 31 and 32 as necessary
33	9.99ns WIDTH R50			RCL 1033	R50	99.9ns ± .1ns	
34	9.99ms DELAY R15	COUNTER set to make delay measurements	FUNC OUT terminate with 50 ohms SYNC OUT terminate with 50 ohms	RCL 1034	R15	9.99ms ± .01ms	
35	1ms DELAY R14	COUNTER	FUNC OUT and SYNC OUT	RCL 1035	R21	1.00ms ± .001ms	Repeat steps 34 and 35 as necessary.
36	9.99μs DELAY R14			RCL 1036	R14	9.99μs ± .01μs	
37	1.04μs DELAY C31			RCL 1037	C31	1.04μs ± .001μs	Repeat steps 36 and 37 as necessary.
38	139ns DELAY R13			RCL 1038	R13	139ns ± .1ns	

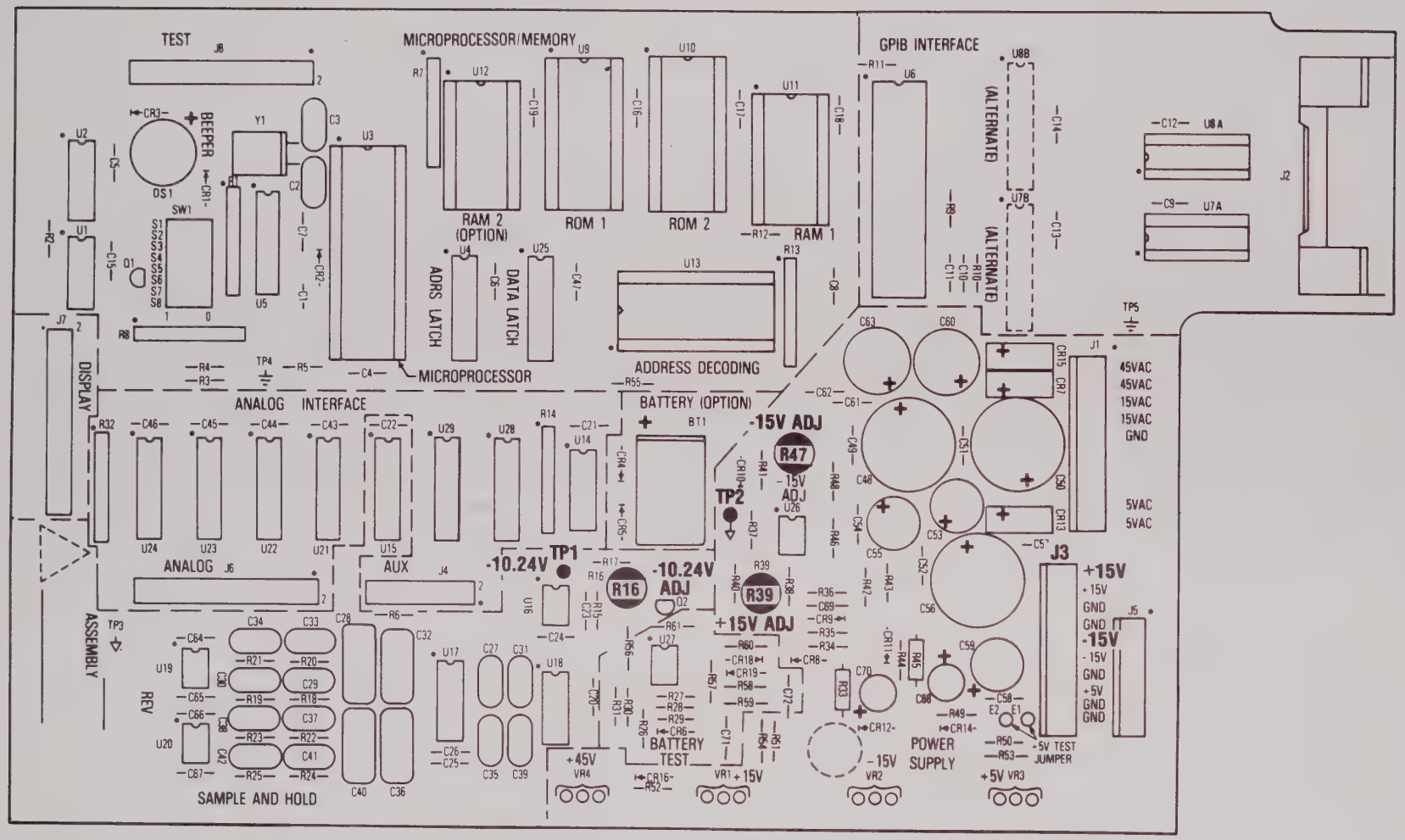


Figure 5-1. Microprocessor/Power Supply Calibration Point Locations

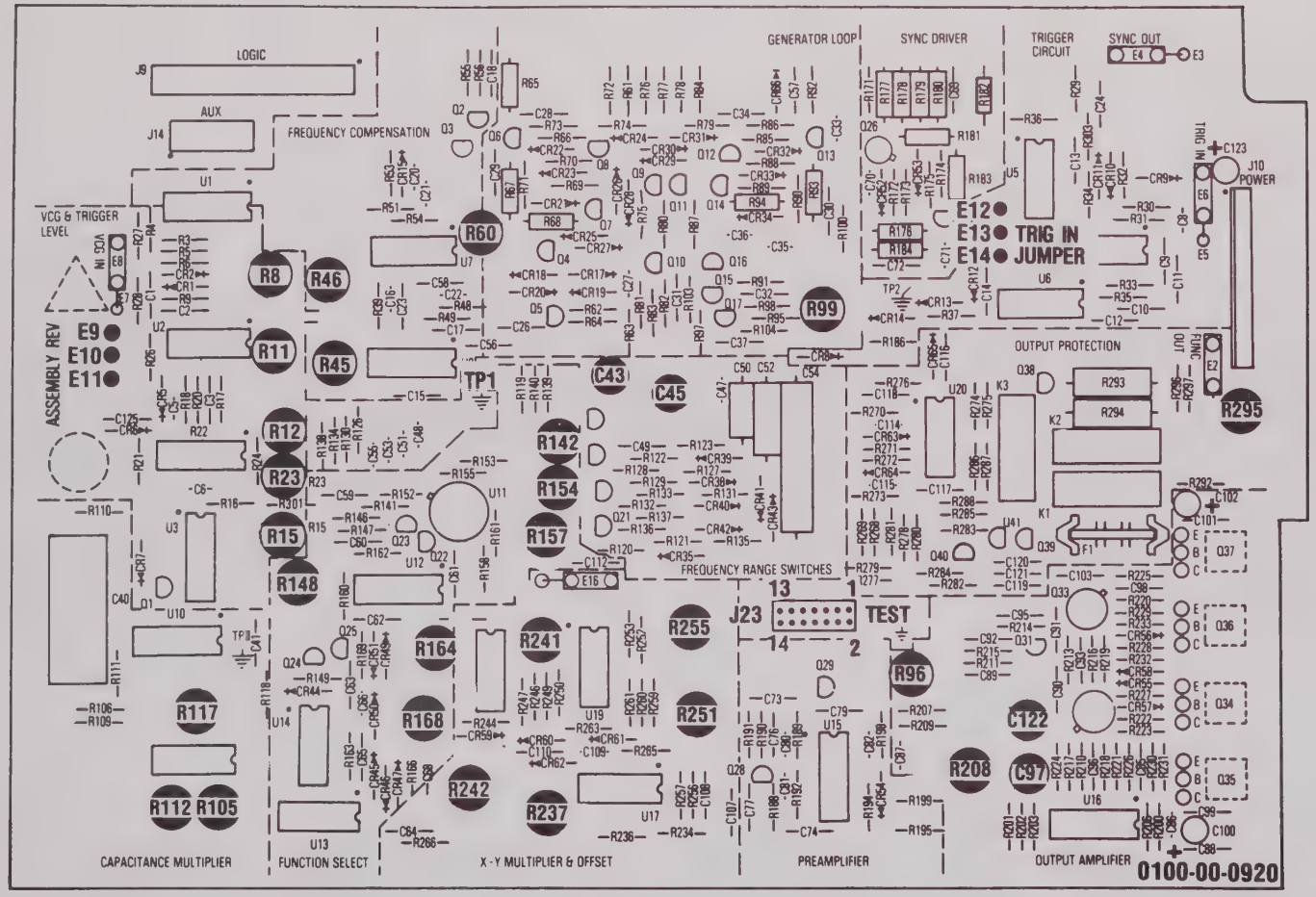


Figure 5-2. Function Generator Calibration Point Locations

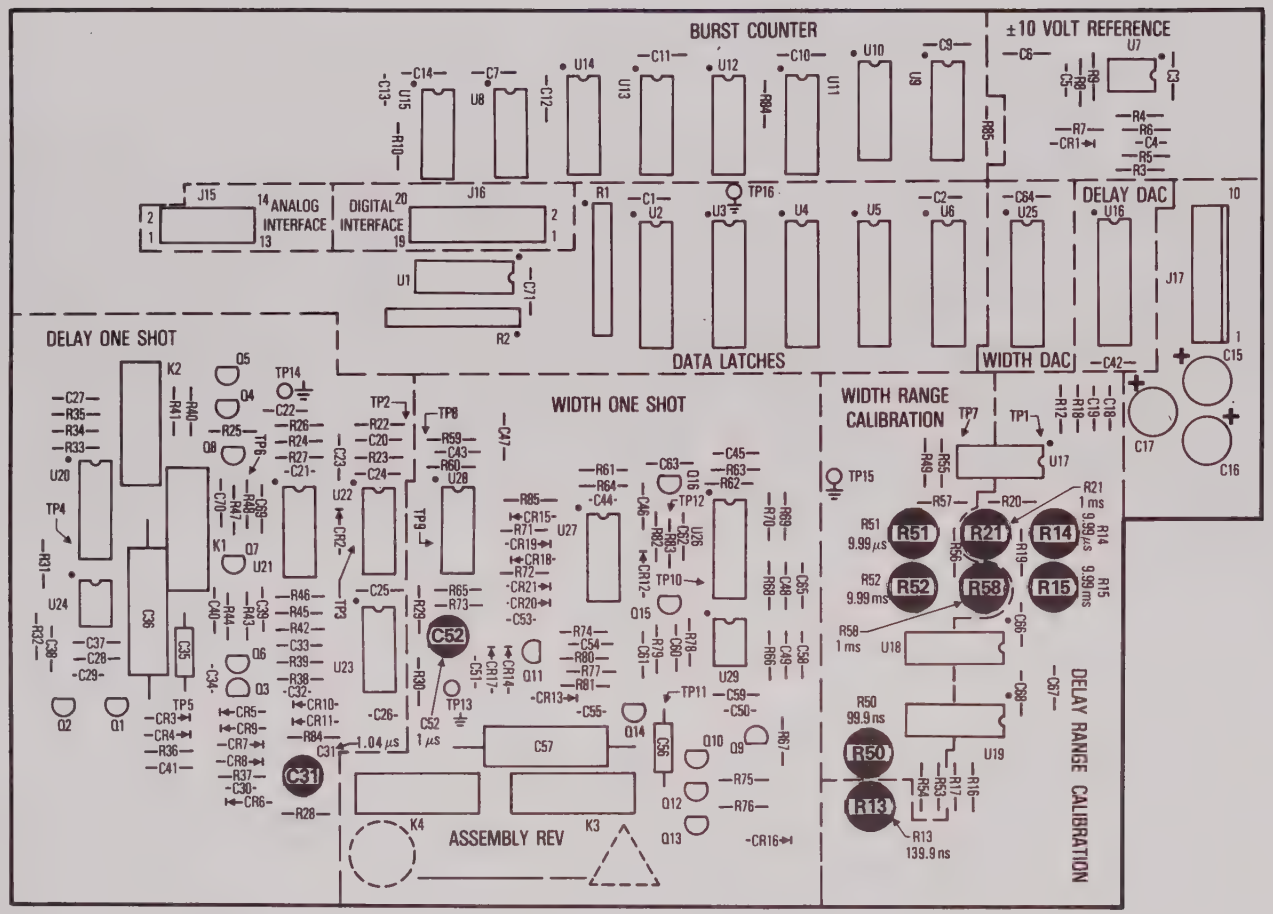


Figure 5-3. Pulse Board Calibration Point Locations

SECTION 6
TROUBLESHOOTING

6.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

6.2 BEFORE YOU START

Since no troubleshooting guide can possibly cover all the potential problems, the aim of this guide is to give a methodology which, if applied consistently, will lead to the problem area. Therefore, it is necessary to familiarize yourself with the instrument by reviewing the functional description and the detailed circuit description in conjunction with the schematic. Successful troubleshooting depends upon understanding the circuit operation within each functional block as well as the block relationships.

6.3 TROUBLESHOOTING

Table 6-1 gives an index of common symptoms. For each symptom a troubleshooting step is referenced that will aid in the solution of the problem. Individual component troubleshooting is given in paragraph 6.4 recommended test equipment is given in paragraph 5.2 and circuit schematics are in the back of this manual.

In all problems:

1. Double check for proper parameter settings.
2. Verify power supplies are in specification.
3. Calibrate or rule out calibration as a problem.
4. Inspect components, wiring and circuit boards for heat damage.
5. Recalibrate as necessary after circuit repair.

Find the instrument symptom in table 6-1 and proceed as directed to the proper troubleshooting step. After verifying the referenced step is okay, proceed to the following step unless directed otherwise.

Table 6-3 provides voltages and waveforms for circuits on the Function Generator Board. These measurements were made with the default instrument parameters

Table 6-1. Symptoms

Symptom	Table 6-2 Step
Display does not light	1.1-1.3
Display is not "WAVETEK 271" at power up	2
"BATTERY LOW" displayed	3
Keyboard has no effect	4
Cannot recall stored settings	5
Won't work on GPIB	6
Keyboard will not work with unit on GPIB	7
No output or incorrect output at FUNC OUT (output on)	8
No output or incorrect frequency	8.1
High frequency incorrect, sine distortion excessive at low frequencies, or no output	8.2
Sine distortion excessive, no output, or no sync output	8.3
No output or frequency incorrect below 100 Hz	8.4
Excessive sine distortion, amplitude errors, or no output	8.5
Offset errors or no output	8.6
Output offset or no output	8.7
No triangle out	9
No square out	10
Trigger or gated mode error	11
No burst or incorrect burst count	12
No pulse output	13
No delayed pulse	14
Incorrect pulse delay	16
Incorrect pulse width	17

automatically selected at power-on or after pressing the RESET key, except that the output is turned on (OUT 1).

Tables 6-4 through 6-10 are truth tables of the logic states for the lines controlling frequency ranges, output relays, waveform functions, trigger modes, trigger slope, pulse delay and pulse width.

6.4 TROUBLESHOOTING INDIVIDUAL COMPONENTS

6.4.1 Transistor

1. A transistor is defective if more than one volt is measured across its base-emitter junction in the forward direction.
2. A transistor when used as a switch may have a few volts reverse bias voltage across base emitter junction.
3. If the collector and emitter voltages are the same, but the base emitter voltage is less than 500mV forward voltage (or reversed bias), the transistor is defective.
4. A transistor, when used as a linear amplifier, is defective if its base current is larger than 10% of its emitter current (calculate currents from voltage across the base and emitter series resistors).
5. In a transistor differential pair (common emitter stages), either their base voltages are the same in normal operating condition, or the one with less forward voltage across its base emitter junction should be off (no collector current); otherwise, one of the transistors is defective.

6.4.2 Diode

A diode (except a zener) is defective if there is greater than one volt (typically 0.7 volt) forward voltage across it.

6.4.3 Operational Amplifier

1. The "+" and "−" inputs of an operational amplifier will generally have less than 15 mV voltage difference when operating under normal conditions except when used as a comparator.
2. When the output of the amplifier is connected to the "−" input (voltage follower connection), the output should be the same voltage as the "+" input voltage; otherwise, the operational amplifier is defective.
3. If the output voltage stays at maximum positive, the "+" input voltage should be more positive than "−" input voltage, or vice versa; otherwise, the operational amplifier is defective.

6.4.4 FET Transistor

1. No gate current should be drawn by the gate of a FET transistor. If so, the transistor is defective.
2. The gate-to-source voltage for a junction FET (JFET) is always reverse biased under a normal operating condition; e.g., the source voltage is more positive than the gate voltage for a N-Channel JFET such as 2N5485, and the source voltage is more negative than gate voltage for a P-Channel JFET such as 2N5462. Otherwise, the FET is defective.

6.4.5 Capacitor

1. Shorted capacitors have zero volts across their terminals.
2. Opened capacitor can be located (but not always) by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.

6.4.6 Digital TTL IC's (e.g. 7400 Series)

1. The device is operating correctly if the output high state is $>+2.4$V and low state is $<+0.5$V.
2. The input must show the same two levels as in step 1. If the levels are between $+0.8$V and $+2.0$V, the connection to the driving circuit output is open.

Table 6-2. Troubleshooting

Step	Symptom	Check	Circuit Description Paragraph	Major Components	Schematic (No./Sheet/ Location)	Remarks
1.1	Display does not Light	AC Power a. Power Source b. Power Cord c. Power Fuse d. Power Selection e. Power Switch	— — — — — —	— — — — — —	— — — Rear panel Rear panel Inside rear panel	
1.2		DC Power a. +45V supply b. +5V supply c. ±15V supply	 4.2.6.2 4.2.6.1 4.2.6.3	 VR4, CR15-16, C60,63 VR3, CR13-14, C56,59 VR1-2, CR7-12, U26, C48,50,53,55	 1094/3/A4-7 1094/3/B4-7 1094/3/D3-7	
1.3		Display a. Supply Voltages b. Filament Driver c. Segment and Digit Drivers d. Fluorescent Display	 4.3.1	 J11 U8, CR3-4, C14-15 U1-5, CR1-2 V1	 0921/1/C7 0921/1/C3 0921/1/C4-7 0921/1/C1-2	
2	Does not display "WAVETEK 271" at power-up	Microprocessor section a. Reset Circuit b. E-clock c. Address Strobe (AS) d. Address/Data Bus (AD) e. Address Bus (ADR) f. Microprocessor Software	 4.2.3 4.2.1.1 4.2.1.1 4.2.1.1 4.2.1.2 4.2.7	 U3,27, CR1-2, 18-19 U3, 6, 13, 25 U3, 4 U3,4-6,9-12 U3-4,6,9-15,28 U9-10	 1094/1/C7, 2/A3 1094/1/D6 1094/1/D6 1094/1/C6 1094/1/C6 —	If okay return to step 1
3	"BATTERY LOW" displayed	Battery Backup a. Battery below 2.4V b. Battery Test Circuit	4.2.3	 BT1, CR4, 5 U27, CR6	 1094/1/A3 1094/2/A3	If okay return to step 2
4	Keyboard has no effect	Keyboard a. ♪ key b. LCL key c. Keyboard d. Keyboard decoder	 4.3.2 4.3.2 4.3.2 4.3.2	 Keyboard Keyboard Keyboard U6,7	 Front panel Front panel 0921/1/B4 0921/1/A3-6	If okay return to step 2
5	Cannot recall stored settings	Stored Settings a. Battery backup b. Reset	4.2.3	 BT1, U12 U27, CR18, 19	 1094/1/A3-4 1094/2/A3	If okay return to step 2
6	Won't work on GPIB	GPIB a. Address switch b. Remote indicator c. Command recall	 4.2.1.8 4.2.2 4.2.2	 SW1, U5 U6-8 U6-8	 1094/1/C5 1094/1/C3 1094/1/C3	If okay return to step 2
7	Keyboard will not work with unit on GPIB	Local Lockout a. Verify remote indicator (R) not displayed b. Verify local lockout not set		 LCL key GTL command	 Front panel GPIB	If okay return to step 6

Table 6-2. Troubleshooting (Continued)

Step	Symptom	Check	Circuit Description Paragraph	Major Components	Schematic (No./Sheet/ Location)	Remarks
8	No or incorrect output at FUNC OUT (output on)	Test Connector: See Remarks				RESET instrument with output on. If bad, refer to:
		a. J23 pin 11 VCGTST = 0.0 ± 0.1 Vdc			0920/3/B1	step 8.1
		b. J23 pin 9 DCCOMP = 0.0 ± 5.0 Vdc			0920/3/B1	step 8.2
		c. J23 pin 7 TRITST = 0.0 ± 0.1 Vdc			0920/3/B1	step 8.3
		d. J23 pin 13 AMPLDC = 5.0 ± 0.2 Vdc			0920/3/B1	step 8.5
		e. J23 pin 1 PATEST = 0.0 ± 0.1 Vdc			0920/3/B1	step 8.6 If okay go to step 8.7
8.1	No output or incorrect frequency	VCG				
		a. SH0 (FRQ input)	4.2.5.3	U15-19, C28	1094/2/C2	
		b. VCG Amp & Compensation	4.4.1	U1-2, CR1-2	0920/1/C4	
		c. Current Sources	4.4.1	U2-3, Q1, CR4-6	0920/1/C4	
8.2	High frequency incorrect, sine distortion excessive at low frequencies or no output.	Frequency Compensation				
		a. DC Amplifier	4.4.5	U7-8, C17,58	0920/2/C6	
		b. High Frequency Comp	4.4.5	U1, U7-8, Q2-3, CR15-16	0920/2/C6	
8.3	Sine distortion excessive, no output, or no sync output	Main Generator				
		a. Current Switch	4.4.2	Q4-5, CR17-20	0920/2/D4	
		b. Switch Buffer	4.4.2	Q6-7, CR21-23	0920/2/C4	
		c. Comparator	4.4.2	Q8-12, CR24-31	0920/2/C3	
		d. Square Buffer	4.4.2	Q13-14, CR32-34	0920/2/C2	
		e. Triangle Buffer	4.4.2	Q15-17, CR66	0920/2/C1	
		f. Frequency Range Switches	4.4.3	Q18-21, CR35-43, C43-47, 50, 52, 54	0920/2/B2-4	
		g. Sync Driver	4.4.6	Q26-27, CR52-53	0920/3/C3-D3	
8.4	No output, or frequency incorrect below 100 Hz	Capacitance Multiplier	4.4.4	U8-11, C40	0920/2/A6-7	
8.5	Excessive sine distortion and amplitude errors, or not output	Amplitude Control				
		a. SH1 (AMP)	4.2.5.3	U15-19, C32	1094/2/C2	
		b. Sine Converter	4.4.8	U11-12, Q22-23, R145	0920/3/C4-6	
		c. XY Multiplier	4.4.9	U17-19, CR59-62	0920/4/A5-8	
8.6	Offset Errors or no output	Preamplifier	4.4.10	U15, Q28-29, CR54	0920/4/C5-7	
8.7	Output offset or no output	Output				
		a. SH2 (OST)	4.2.5.3	U15-18,20, C36	1094/2/C2	
		b. Offset	4.4.9	U17	0920/4/B5	
		c. Output Amplifier	4.4.11	U16, Q30-37, CR55-58	0920/4/C1-5	
		d. Fuse and Fuse Sense	4.4.12.2	U20, F1	0920/4/B1-2	
		e. Overvoltage Sense	4.4.12.1	U20, CR63-65	0920/4/B4	
		f. Output Attenuator	4.4.12.3	Q38-41, K1-3	0920/4/B1-2	

Table 6-2. Troubleshooting (Continued)

Step	Symptom	Check	Circuit Description Paragraph	Major Components	Schematic (No./Sheet/ Location)	Remarks
9	No triangle out	Triangle Level	4.4.8	U12, Q24-25	0920/3/B5-6	If okay return to step 8.3
10	No square out	Square				
		a. Square Logic	4.4.8	U13-14	0920/3/B5-6	If okay return to step 8.3d
		b. Square Shaper	4.4.8	U12, CR45-51	0920/3/A3-4	
11	Trigger or gated mode error	Trigger Circuit				
		a. SH3 (TRL)	4.2.5.3	U15-18,20, C40	1094/2/B2-3	If okay return to step 8.1c
		b. Trigger Level Amplifier	4.4.1	U2	0920/1/B6	
		c. Trigger Comparator	4.4.7	U4, CR9-11	0920/1/B5	
		d. Mode Logic	4.4.7	U5-6, CR7-8,12-14	0920/1/B4	
12	No burst or incorrect burst count	Burst Counter				
		a. Auxiliary Buffers	4.2.4.3	U28-39	1094/2/B6-7	
		b. Auxiliary Connectors		cables	connectors	
		c. TRIG IN Jumpers	4.4.7	E13-E14	0920/1/A4	
		d. Program Decode	4.5.1	U1	0991/1/C7	
		e. Program Registers	4.5.1	U2-U4	0991/1/C5, C6	
		f. Burst Mode Logic	4.5.2	U8, U15	0991/1/B1, B2, C1, C7, B7	
		g. Preset Counter	4.5.2	U9-U13	0991/1/B3-B6	
13	No pulse output	Data Registers	4.5.1	U2	0991/1/C6	Check logic states of DELON and $\overline{\text{DELPLS}}$ lines.
		Delay one-shot	4.5.4.1			Delay one-shot circuit is probably OK if pulse is present on DELTOWID line.
		a. Comparator Logic	4.5.4.1.7	U21A, U21B, U22A, U22B, U20D	0991/2/C3, C4, D3	
		b. Double Pulse Logic	4.5.4.1.8	U23A, U23D	0991/2/C2, D2	
		c. 3-Decade Current Source	4.5.4.1.1	U24A, Q1, Q2, U20A, U20B, U20C	0991/2/A7, B7	
		d. Ramp Reset Circuit	4.5.4.1.3	Q3, CR3-CR5, CR7-CR11	0991/2/B5, B6	
		e. Range Capacitors Circuit	4.5.4.1.2	Q4, Q5, K1, K2	0991//2/A3, B3	
		f. FET Buffer	4.5.4.1.4	Q6-Q8, U24B	0991/2/B2, B3	
		g. Delay DAC	4.5.4.1.5	U16, U17A	0991/2/C6, C7, D6, C7	
		h. Delay Range Calibration Circuit	4.5.4.1.6	U17D, U18A, U18D, U19A, U19D	0991/2/C4, C5, D4, D5	
		Width One-Shot	4.5.4.2			
		a. Comparator Logic	4.5.4.2, 4.5.4.1.7	U27A, U27B, U28A, U28B, U26D	0991/3/C3, C4, D3	
		b. 3-Decade Current Source	4.5.4.2, 4.5.4.1.1	U29B, Q9, Q10, U26A, U26B, U26C	0991/3/A7, B7	
		c. Ramp Reset Circuit	4.5.4.2, 4.5.4.1.3	Q11, CR13-CR15, CR17-CR21	0991/3/B5, B6	
		d. Range Capacitors Circuit	4.5.4.2, 4.5.4.1.2	Q12, Q13, K3, K4	0991/3/A3, B3	
		e. FET Buffer	4.5.4.2, 4.5.4.1.4	Q14-Q16, U29A	0991/3/B2, B3	
		f. Width DAC	4.5.4.2, 4.5.4.1.5	U25, U17B	0991/3/C6, D6, D7	
		g. Width Range Calibration Circuit	4.5.4.2, 4.5.4.1.6	U17C, U18B, U18C, U19B, U19C	0991/3/C4, C5, D4, D5	

Table 6-2. Troubleshooting (Continued)

Step	Symptom	Check	Circuit Description Paragraph	Major Components	Schematic (No./Sheet/ Location)	Remarks
14	No delayed pulse (undelayed pulse OK)	Data Registers	4.5.1	U2	0991/1/C6	Check logic states of DELON and $\overline{\text{DELPLS}}$ lines.
		Delay one-shot	4.5.4.1			
		a. Comparator Logic	4.5.4.1.7	U21A, U21B, U22A, U22B, U20D	0991/2/C3, C4, D3	
		b. Double Pulse Logic	4.5.4.1.8	U23A, U23D	0991/2/C2, D2	
		c. 3-Decade Current Source	4.5.4.1.1	U24A, Q1, Q2, U20A, U20B, U20C	0991/2/A7, B7	
		d. Ramp Reset Circuit	4.5.4.1.3	Q3, CR3-CR5, CR7-CR11	0991/2/B5, B6	
		e. Range Capacitors Circuit	4.5.4.1.2	Q4, Q5, K1, K2	0991/2/A3, B3	
		f. FET Buffer	4.5.4.1.4	Q6-Q8, U24B	0991/2/B2, B3	
		g. Delay DAC	4.5.4.1.5	U16, U17A	0991/2/C6, C7, D6, D7	
		h. Delay Range Calibration Circuit	4.5.4.1.6	U17D, U18A, U18D, U19A, U19D	0991/2/C4, C5, D4, D5	
15	No double pulse	Data Registers	4.5.1	U2	0991/1/C6	Check logic states of DELON and $\overline{\text{DELPLS}}$ lines.
		Double Pulse Logic	4.5.4.1.8	U23A, U23D	0991/2/C2, D1	
16	Incorrect pulse delay	Data Registers	4.5.1, Table 4-2	U5, U6	0991/1/C6	Check logic states of delay range control lines (Table 6-9).
		Delay one-shot	4.5.4.1			
		a. Comparator Logic	4.5.4.1.7	U21A, U21B, U22A, U22B, U20D	0991/2/C3, C4, D3	
		b. Double Pulse Logic	4.5.4.1.8	U23A, U23D	0991/2/C2, D2	
		c. 3-Decade Current Source	4.5.4.1.1	U24A, Q1, Q2, U20A, U20B, U20C	0991/2/A7, B7	
		d. Ramp Reset Circuit	4.5.4.1.3	Q3, CR3-CR5, CR7-CR11	0991/2/B5, B6	
		e. Range Capacitors Circuit	4.5.4.1.2	Q4, Q5, K1, K2	0991/2/A3, B3	
		f. FET Buffer	4.5.4.1.4	Q6-Q8, U24B	0991/2/B2, B3	
		g. Delay DAC	4.5.4.1.5	U16, U17A	0991/2 C6, C7, D6, D7	
		h. Delay Range Calibration Circuit	4.5.4.1.6	U17D, U18A, U18D, U19A, U19D	0991/2/C4, C5, D4, F5	
		Circuit Calibration				Section 5 of manual.

Table 6-2. Troubleshooting (Continued)

Step	Symptom	Check	Circuit Description Paragraph	Major Components	Schematic (No./Sheet/ Location)	Remarks
17	Incorrect pulse width	Data Registers	4.5.1, Table 4-3	U5, U6		Check logic states of width range control lines (Table 6-10).
		Width one-shot	4.5.4.2			
		a. Comparator Logic	4.5.4.2, 4.5.4.1.7	U27A, U27B, U28A, U28B, U26D	0991/3/C3, C4, D3	
		b. 3-Decade Current Source	4.5.4.2, 4.5.4.1.1	U29B, Q9, Q10, U26A, U26B, U26C	0991/3/A7, B7	
		c. Ramp Reset Circuit	4.5.4.2, 4.5.4.1.3	Q11, CR13-CR15, CR17-CR21	0991/3/B5, B6	
		d. Range Capacitors Circuit	4.5.4.2, 4.5.4.1.2	Q12, Q13, K3, K4	0991/3/A3, B3	
		e. FET Buffer	4.5.4.2, 4.5.4.1.4	Q14-Q16, U29A	0991/3/B2, B3	
		f. Width DAC	4.5.4.2, 4.5.4.1.5	U25, U17B	0991/3/C6, D6, D7	
		g. Width Range Calibration Circuit	4.5.4.2, 4.5.4.1.6	U17C, U18B, U18C, U19B, U19C	0991/3/C4, C5,	
		Circuit Calibration				Section 5 of manual.

Table 6-3. Function Generator Board Voltages (Reset Condition)

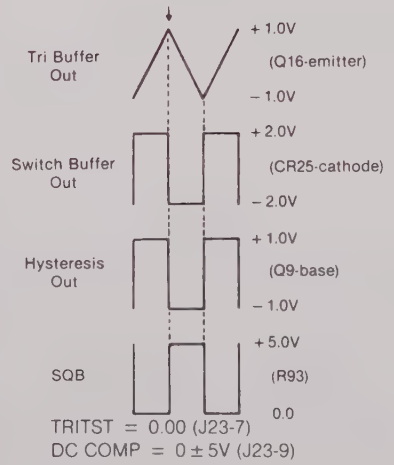
Circuit	Control Voltages	Circuit Voltages
VCG and trigger level	$\overline{OVR}$ = TTL high (J9-19) $\overline{FR5}$ = TTL high (J9-10) FRQ = 1.00V (J9-1) TRL = +4.25V (J9-4)	TLO = +1.5V (U2-7) THC = +1.2V (U3-9) VCV = −0.4V (E10) VCGTST = 0.00 Vdc (J23-11)
Frequency compensation	$\overline{FR7}$ = TTL high (J9-12) $\overline{FR6}$ = TTL high (J9-11) $\overline{FR5}$ = TTL high (J9-10) $\overline{DCA}$ = TTL low (J9-18)	DC COMP = 0 ± 5V (U7-14)
Generator loop		

Table 6-3. Function Generator Board Voltages (Reset Condition) (Continued)

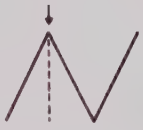
Circuit	Control Voltages	Circuit Voltages
Frequency range	$\overline{FR3}$ = TTL high (J9-8) $\overline{FR4}$ = TTL low (J9-9) $\overline{FR5}$ = TTL high (J9-10) $\overline{FR6}$ = TTL high (J9-11)	
Capacitance multiplier	$\overline{FR0}$ = TTL high (U10-9) $\overline{FR1}$ = TTL high (U10-8) $\overline{FR2}$ = TTL low (U10-1) $\overline{CPM}$ = TTL high (U10-16)	TRB +1.0V −1.0V
Trigger circuit	+TR = TTL high (J9-22) −TR = TTL low (J9-21) MC0 = TTL low (J9-16) MC1 = TTL low (J9-17)	TLO = +1.5V (R29) THC = +1.2V (CR14-cathode) SQB = +5.0V 0.0V (U5-4)
Function select	SQR = TTL low (U14-1) $\overline{SQR}$ = TTL low (U14-10) PLS = TTL low (U14-2) $\overline{PLS}$ = TTL low (U14-5) EXW = TTL low (U13-12) $\overline{SIN}$ = TTL low (R141) $\overline{TRI}$ = TTL high (R149) $\overline{RCT}$ = TTL high (R170)	TRB  +1.0V (R139/140) −1.0V
X-Y multiplier and offset		OST = +5.00V (R235) Amp out = 0.0 Vdc (U17-8) AMP = +5.00V (R266) AMPLDC = +5.00V (J23-13)
Preamplifier		Preamp out +0.75 CR54-anode) −0.75 PATEST = 0.0 Vdc (J23-1)
Output amplifier		Off amp out = 0.0 Vdc (R207) Preamp out +0.75 (R209) −0.75 PATEST = 0.0 Vdc (J23-1) Out amp out +5.0V (R231/232) −5.0V

Table 6-3. Function Generator Board Voltages (Reset Condition) (Continued)

Circuit	Control Voltages	Circuit Voltages
Output protection	FUB = TTL low (J9-34) OAP = TTL low (J9-33) OA0 = TTL low (J9-13) OA2 = TTL low (J9-15)	Fuse sense input +5.0V (F1) −5.0V

Table 6-4. Frequency Truth Table

Frequency Range	$\overline{FR0}$	$\overline{FR1}$	$\overline{FR2}$	$\overline{FR3}$	$\overline{FR4}$	$\overline{FR5}$	$\overline{FR6}$	$\overline{FR7}$	$\overline{CPM}$	$\overline{OVR}$	$\overline{DCA}$
10.0 – 99.9 mHz	1	1	1	0	1	1	1	1	0	1	1
100 – 999 mHz	0	1	1	0	1	1	1	1	0	1	1
1.00 – 9.99 Hz	1	0	1	0	1	1	1	1	0	1	1
10.0 – 99.9 Hz	1	1	0	1	1	1	1	1	0	1	1
100 – 999 Hz	1	1	0	0	1	1	1	1	1	1	0
1.00 – 9.99 kHz	1	1	0	1	0	1	1	1	1	1	0
10.0 – 99.9 kHz	1	1	0	1	1	0	1	1	1	1	0
100 – 999 kHz	1	1	0	1	1	1	0	1	1	1	0
1.00 – 9.99 MHz	1	1	0	1	1	1	1	0	1	1	0
10.0 – 12.0 MHz	1	1	0	1	1	1	1	0	1	0	0

Table 6-5. Output Relay Truth Table

Condition	OA0	OA2	OA1
Ampl + |Ofst| > 1.00V, Output On	1	0	1
Ampl + |Ofst| ≤ 1.00V, Output On	1	1	0
Output Off, Hi Z (~539 kΩ)	0	0	1
Output Off, Lo Z (~55.6Ω)	0	1	0

Table 6-6. Function Truth Table

Function	$\overline{SIN}$	$\overline{TRI}$	$\overline{RCT}$	SQR	$\overline{SQR}$	PLS	$\overline{PLS}$	EXW	
Sine	0	1	1	0	0	0	0	0	
Triangle	1	0	1	0	0	0	0	0	
Square	1	1	0	1	0	0	0	0	
Sqr Comp	1	1	0	0	1	0	0	0	
DC	1	1	1	0	0	0	0	0	
Ext Width	1	1	0	0	0	0	0	1	
Single Pulse	1	1	0	0	0	1	0	0	
Delayed Pulse	1	1	0	0	0	1	0	0	
Double Pulse	1	1	0	0	0	1	0	0	
Single Pulse Complement	1	1	0	0	0	0	1	0	
Delayed Pulse Complement	1	1	0	0	0	0	1	0	
Double Pulse Complement	1	1	0	0	0	0	1	0	

Table 6-7. Mode Truth Table

Mode	MC0	MC1	
Cont	0	0	
Trig	1	0	
Gate	1	1	(Includes Burst Mode)

Table 6-8. Trigger Truth Table

Trigger	+TR	−TR	
+ (Rising)	1	0	
− (Falling)	0	1	
Man Trig	1	1	

Table 6-9. Pulse Delay Ranges

Delay Range	Control Line Logic States							
	DR0	DR1	DR2	DR3	DR4	DR5	DR6	DR7
80 ns-139 ns	L	H	H	L	H	H	L	H
140 ns-1.03 μs	L	H	L	H	H	L	H	H
1.04 μs-9.99 μs	L	H	H	H	L	H	H	H
10 μs-99.9 μs	H	L	H	H	H	L	H	H
100 μs-999 μs	H	L	H	H	L	H	H	H
1 ms-9.99 ms	H	L	H	H	H	L	H	L
10 ms-99.9 ms	H	L	H	H	L	H	H	L

Table 6-10. Pulse Width Ranges

Width Range	Control Line Logic States							
	WR0	WR1	WR2	WR3	WR4	WR5	WR6	WR7
40 ns-99.9 ns	L	H	H	L	H	H	L	H
100 ns-999 ns	L	H	L	H	H	L	H	H
1 μs-9.99 μs	L	H	H	H	L	H	H	H
10 μs-99.9 μs	H	L	H	H	H	L	H	H
100 μs-999 μs	H	L	H	H	L	H	H	H
1 ms-9.99 ms	H	L	H	H	H	L	H	L
10 ms-99.9 ms	H	L	H	H	L	H	H	L

SECTION 7
PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings, parts lists and schematics are in the arrangement shown below.

7.2 ADDENDA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to summarize the changes made and are inserted immediately inside the rear cover. If no such pages exist, the manual is correct as printed.

7.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit, and, if applicable, the function performed.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

DRAWING	DRAWING NUMBER
Instrument Overall Dimensions (270 Series)	0009-00-0180
Instrument Schematic	0004-00-0180
Instrument Parts List	1000-00-0184
Chassis Assembly	0102-00-0922
Chassis Parts Lists	1101-00-0922
Front Panel Assembly	0102-00-0923
Front Panel Parts List	1101-00-0999
Display Schematic	0103-00-0921
Display Assembly	1100-00-0921
Display Parts List	1100-00-0921
Function Generator Schematic	0103-00-0920
Function Generator Assembly	1100-00-0920
Function Generator Parts List	1100-00-0920
Microprocessor/Power Supply Schematic	0103-00-1094
Microprocessor/Power Supply Assembly	1100-00-1094
Microprocessor/Power Supply Parts List	1100-00-1094
Prom Package	1109-00-0020
Pulse Board Schematic	0103-00-0991
Pulse Board Assembly	1100-00-0991
Pulse Board Parts List	1100-00-0991

DRAWING	DRAWING NUMBER
Rear Panel Assembly	0102-00-0924
Rear Panel Parts List	1101-00-0924
Rack Adapter Assembly	0102-00-1043
Rack Adapter Parts List	1101-00-1043
Dual Rack Mount Assembly and Parts List	0102-00-1041
Rack Slide Assembly and Parts List	0102-00-1042
Option 002 Schematic and Parts List	0103-00-1010
Microprocessor/Power Supply Schematic (Serial Numbers Less Than 7230039)	0103-00-0919

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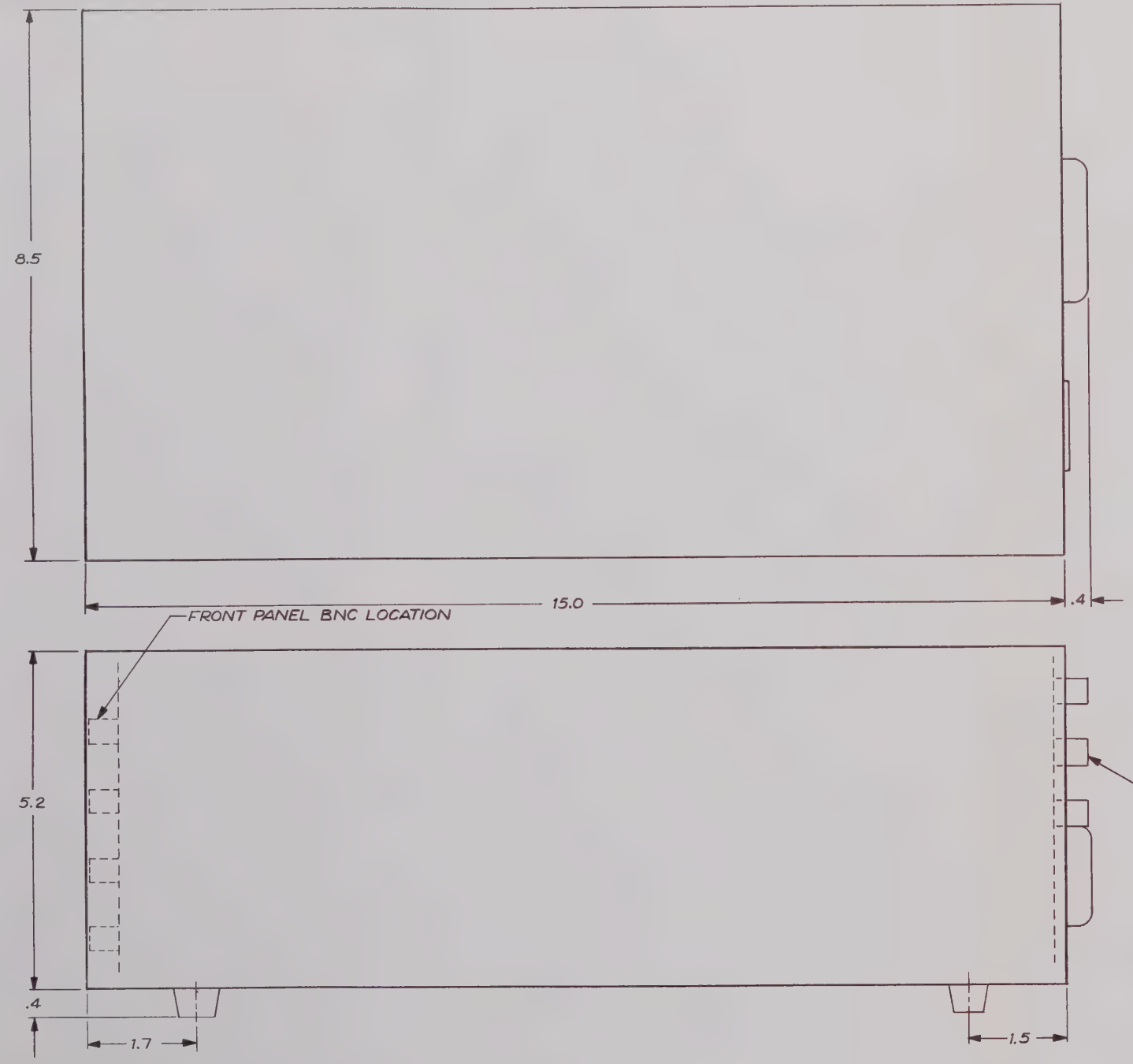
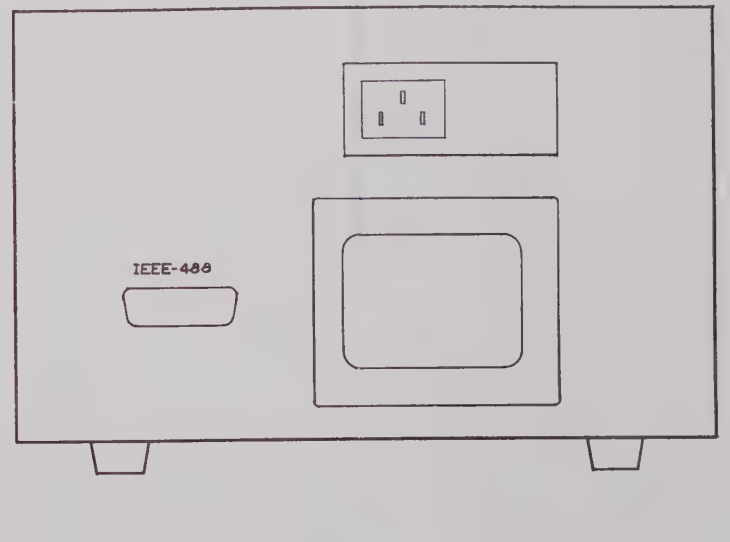
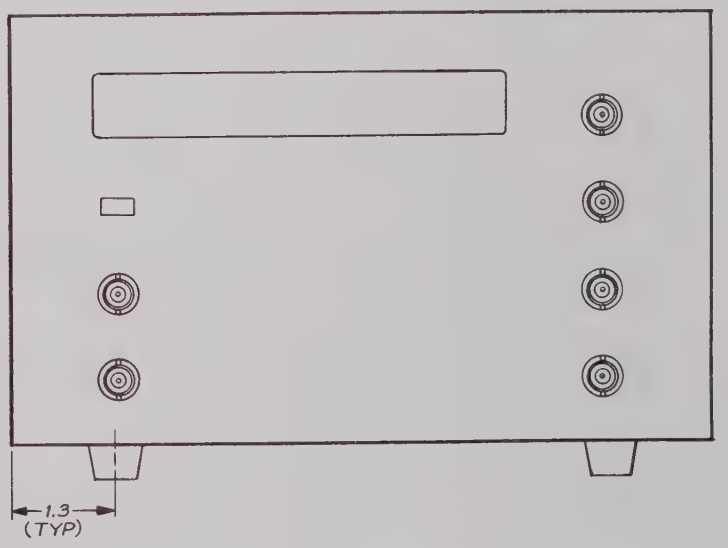
REV	ECN	BY	DATE	APP







NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 3964	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: INSTRUMENT OVERALL DIMENSIONS (270 SERIES)
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO. 0009-00-0180 REV
	SCALE 1/1	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3984

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REV	ECN	BY	DATE	APP
	3369 CLASS III	SC	9 2482	
A	#3904	SC	7-2689	

A5 REAR PANEL ASSY

J2 — IEEE-488

1	D101
2	D102
3	D103
4	D104
5	EOI
6	DAV
7	RFD
8	DAC
9	IFC
10	SRQ
11	ATN
12	
13	D105
14	D106
15	D107
16	D108
17	REN
18	GND
19	GND
20	GND
21	GND
22	GND
23	GND
24	GND

J18 — AC POWER RECP
100-120V ½A SB
220-240 ¼A SB
F1

T1 — 1204-00-0049

W1 / P1 / J1

1	15 VAC
2	15 VAC
3	15 VAC
4	GND
5	—
6	—
7	—
8	5 VAC
9	5 VAC
10	

TEST CONNECTOR

J8

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
E	ADR 15	GND	ADR 14	A5	ADR 13	GND	ADR 12	NMI	ADR 11	GND	ADR 10	GND	ADR 9	GND	ADR 8	GND	AD7	GND	AD6	GND	AD5	TEST	AD4	GND	AD3	+5V	AD2	N.C.	AD1	N.C.	AD0	GND	R/W

A6 µ PROC/POWER SUPPLY BOARD

A2 FRONT PANEL ASSY

J7 / P7 — W4

1	+45V
2	GND
3	+5V
4	+5V
5	+5V
6	+5V
7	+5V
8	KYBD
9	PORT
10	PORT 16
11	DISP/
12	GND
13	AD4
14	AD3
15	AD2
16	AD1
17	AD0
18	ADR 3
19	ADR 2
20	ADR 1
21	ADR 0
22	GND
23	DATA 7
24	DATA 6
25	DATA 5
26	DATA 4
27	DATA 3
28	DATA 2
29	DATA 1
30	DATA 0
31	GND
32	GND
33	GND
34	+5V

J11

A3 DISPLAY BOARD 1100-00-0921

A4 CABLE INTERFACE BOARD

J3 / P3 — J6 / P6

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
+15V	+15V VR	GND	GND	-15V VR	-15V	GND	+5	GND	GND	SHO	SH1	SH2	SH3	ANL 0	ANL 1	ANL 2	ANL 3	ANL 4	ANL 5	ANL 6	ANL 7	ANL 8	ANL 9	ANL 10	ANL 11	ANL 12	ANL 13	ANL 14	ANL 15	ANL 16	ANL 17	ANL 18	ANL 19	ANL 20	ANL 21	ANL 22	ANL 23	ANL 24	ANL 25	ANL 26	ANL 27	PORT 17	PORT 11

W2 — W3

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
KEY	AMP	RST	RF0	RF1	RF2	RF3	RF4	RF5	RF6	RF7	GA 0	GA 1	GA 2	MC 0	MC 1	DCA	SVR	CPM	-12	+12	EXW	SQR	SQR	SIN	TRI	RCT	PLS	PLS			OAP	FUB	

P10 / J10 — P9 / J9

A7 FUNCTION GENERATOR BOARD

TEST CONNECTOR

J23

1	2	3	4	5	6	7	8	9	10	11	12	13	14
PA TEST	+15 VT	-15 VT	GND	+5 VT	GND	TRI TST	GND	DC COMP	GND	VCG TST	GND	AMP LOC	GND

A8 OUTPUT FUSE BOARD

A1 CHASSIS ASSY

J4 / P4 — J5 / P5

W13

1	DATA 0
2	DATA 1
3	DATA 2
4	DATA 3
5	DATA 4
6	DATA 5
7	DATA 6
8	DATA 7
9	ADR 0
10	ADR 1
11	ADR 2
12	ANA 12
13	ANA 13
14	ANA 14
15	GND
16	GND
17	GND
18	GND
19	NOAM PWR
20	PORT 13

W14

1	+15V
2	+15V VR
3	GND
4	GND
5	-15V VR
6	-15V
7	GND
8	+5
9	GND
10	GND

P16 / J16 — P17 / J17

A10 AUXILLARY FUNCTION BOARD

J15 / P15

W15

1	GND
2	VCG1
3	GND
4	VCG2
5	GND
6	GND
7	TRG1
8	GND
9	TRG2
10	GND
11	PLS1
12	GND
13	SGS
14	GND

P14 / J14

MODEL 278 ONLY

P13 / J13

1	E11	W18	J24 REF OUT
2	E12		
3	E10	W19	J25 REF IN
4	E9		

P12 / J12

10	E1	W9	J19 FUNC OUT
9	E2		
8			
7	E4		
6	E3	W10	J20 SYNC OUT
5	E6		
4	E5	W11	J21 TRIG IN
3			
2	E8		
1	E7	W12	J22 VCG IN

E1 E2 E3 E4

FUNC OUT	E1 E2	W5
SYNC OUT	E3 E4	W6
TRIG IN	E5 E6	W7
VCG IN	E7 E8	W8

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN FN AQUINO	DATE 9/29/82	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	PROJ ENGR RBG	2/1K/83	TITLE SCHEMATIC INSTRUMENT
FINISH WAVETEK PROCESS —	RELEASE APPROV BH	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030	
	DO NOT SCALE DWG	SCALE	MODEL NO 270, 271, 278 — DWG NO 0004-00-0180 — REV A
			CODE IDENT 23338 — SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, INSTRUMENT	0004-00-0180	WVTK	0004-00-0180	1
NONE	FINAL CAL PROCEDURE	0006-00-0184	WVTK	0006-00-0184	1
NONE	SPECIFICATIONS	0007-00-0184	WVTK	0007-00-0184	1
NONE	PCA, FUNCTION GEN	270-0920	WVTK	1100-00-0920	1
NONE	PCA, DISPLAY	270-0921	WVTK	1100-00-0921	1
NONE	PCA, CABLE INTERFACE	270-0976	WVTK	1100-00-0976	1
NONE	PCA, PULSE BOARD	270-0991	WVTK	1100-00-0991	1
NONE	PCA, MICRO-PROC/ POWER SUPPLY	273-1094	WVTK	1100-00-1094	1
NONE	ASSY, CHASSIS	270-0922	WVTK	1101-00-0922	1
NONE	ASSY, REAR PANEL	270-0924	WVTK	1101-00-0924	1
NONE	ASSY, FRONT PANEL	270-0999	WVTK	1101-00-0999	1
NONE	PROM PACKAGE	270-0020	WVTK	1109-00-0020	1
NONE	CHASSIS CABLE KIT	270-1000	WVTK	1207-00-1000	1
NONE	INSTRUCTION MANUAL	MANUAL-271	WVTK	1300-00-0184	1
NONE	INSERT	101-6F	WVTK	3300-00-0013	1
NONE	CARTON	101-6A	WVTK	3300-01-0010	1
NONE	PWR CORD	6001-80-0005	WVTK	6001-80-0005	1

WAVETEK PARTS LIST	TITLE MODEL 271 12MHZ PROGRAMMABLE PULSE FUNCTION GENERATOR	ASSEMBLY NO. 1000-00-0184 PAGE: 1	REV C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE PARTS LIST MODEL 271 12 MHz PROGRAMMABLE PULSE FUNCTION GENERATOR
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 271 / DWG NO 1000-00-0184 / REV C
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS
REORDER NO A27008

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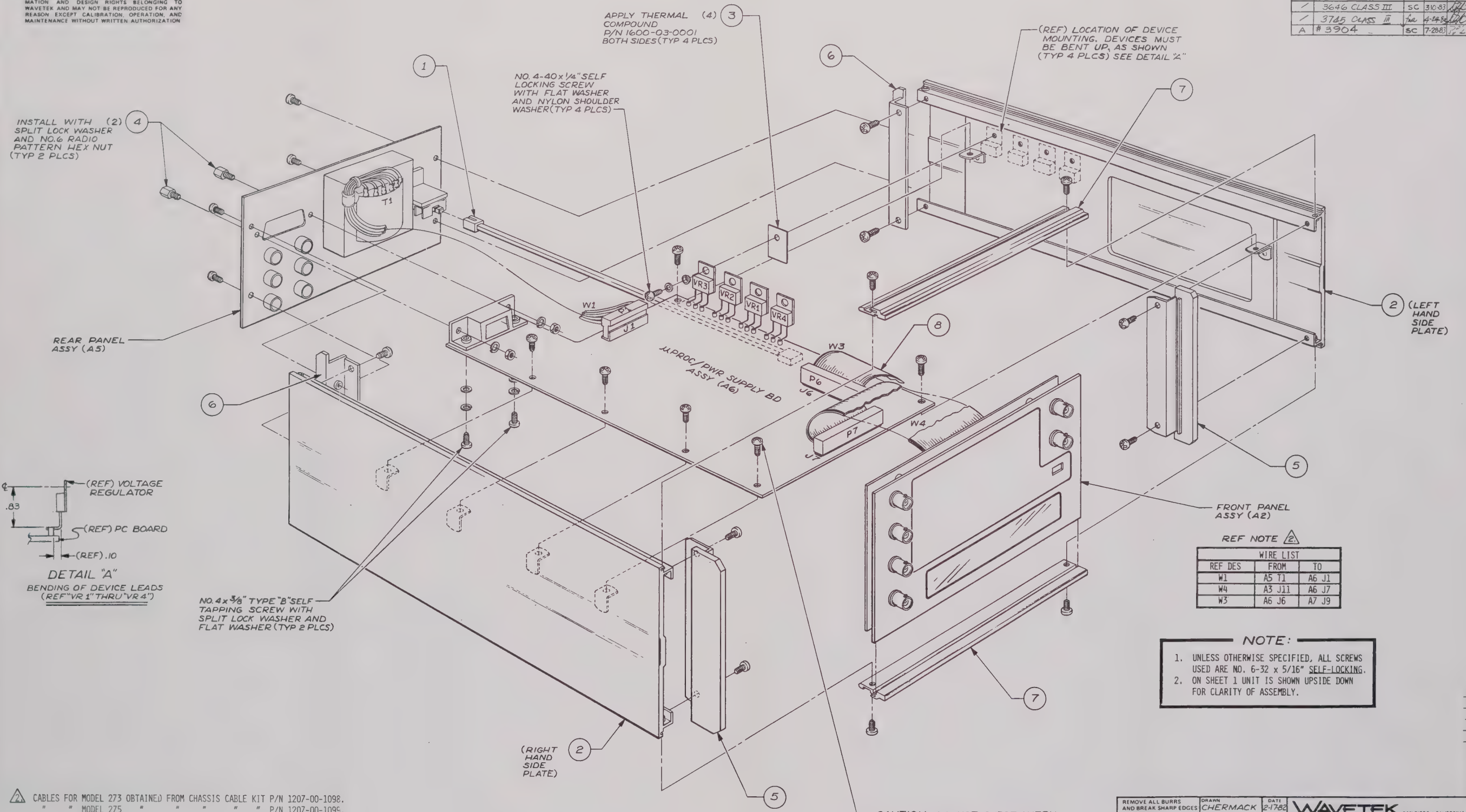
REV	ECN	BY	DATE	APP
/	#3330 CLASS III	SC	9-14-82	
/	3591 CLASS III	SC	2-14-83	
/	3646 CLASS III	SC	3-10-83	
/	3745 CLASS III	SC	4-28-83	
A	#3904	SC	7-28-83	


APPLY THERMAL COMPOUND P/N 1600-03-0001 BOTH SIDES (TYP 4 PLCS)
(4)
3
1
NO. 4-40 x 1/4" SELF LOCKING SCREW WITH FLAT WASHER AND NYLON SHOULDER WASHER (TYP 4 PLCS)
INSTALL WITH (2) SPLIT LOCK WASHER AND NO. 6 RADIO PATTERN HEX NUT (TYP 2 PLCS)
4
(REF) LOCATION OF DEVICE MOUNTING. DEVICES MUST BE BENT UP, AS SHOWN (TYP 4 PLCS) SEE DETAIL "A"
6
7
T1
VR3
VR2
VR1
VR4
W1
P1
J1
REAR PANEL ASSY (A5)
W3
P6
J6
8
A1 PROC/PWR SUPPLY BD ASSY (A6)
W4
P7
J7
2 (LEFT HAND SIDE PLATE)
5
FRONT PANEL ASSY (A2)
(REF) VOLTAGE REGULATOR
.83
(REF) PC BOARD
(REF) .10
DETAIL "A"
BENDING OF DEVICE LEADS (REF "VR 1" THRU "VR 4")
NO. 4 x 3/8" TYPE "B" SELF TAPPING SCREW WITH SPLIT LOCK WASHER AND FLAT WASHER (TYP 2 PLCS)
(RIGHT HAND SIDE PLATE)
CAUTION: DO NOT OVERTIGHTEN THE 6 SCREWS WHICH MOUNT PC BD ASSEMBLY TO SIDE PLATES (TORQUE TO 6 INCH POUNDS)

REF NOTE (2)

WIRE LIST		
REF DES	FROM	TO
W1	A5 T1	A6 J1
W4	A3 J11	A6 J7
W3	A6 J6	A7 J9

NOTE:

1. UNLESS OTHERWISE SPECIFIED, ALL SCREWS USED ARE NO. 6-32 x 5/16" SELF-LOCKING.
2. ON SHEET 1 UNIT IS SHOWN UPSIDE DOWN FOR CLARITY OF ASSEMBLY.

(2) CABLES FOR MODEL 273 OBTAINED FROM CHASSIS CABLE KIT P/N 1207-00-1098.
" " MODEL 275 " " " " " P/N 1207-00-1095.
" " MODEL 270 " " " " " P/N 1207-00-0926
" " MODEL 271 " " " " " P/N 1207-00-1000
" " MODEL 278 " " " " " P/N 1207-00-1004

1. SEE PARTS LIST NO: 1101-00-0922

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 2-17-82	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RBG	7/15/83	TITLE: ASSEMBLY, CHASSIS (A1)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 ANGLES : 1 XX : 030		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO 0102-00-0922 REV A
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 2

BISHOP GRAPHICS ACCUPRESS REORDER NO. A-3894

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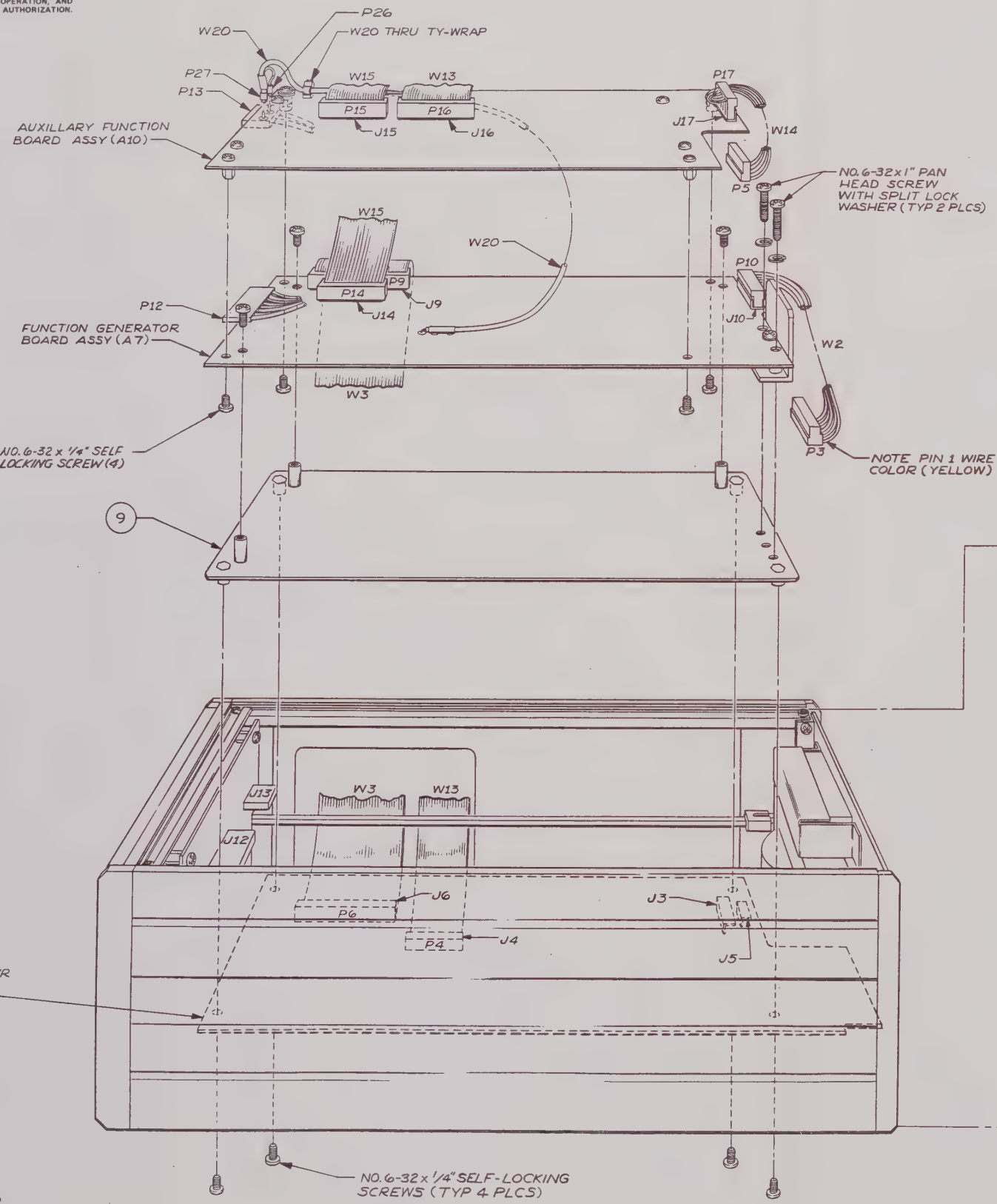
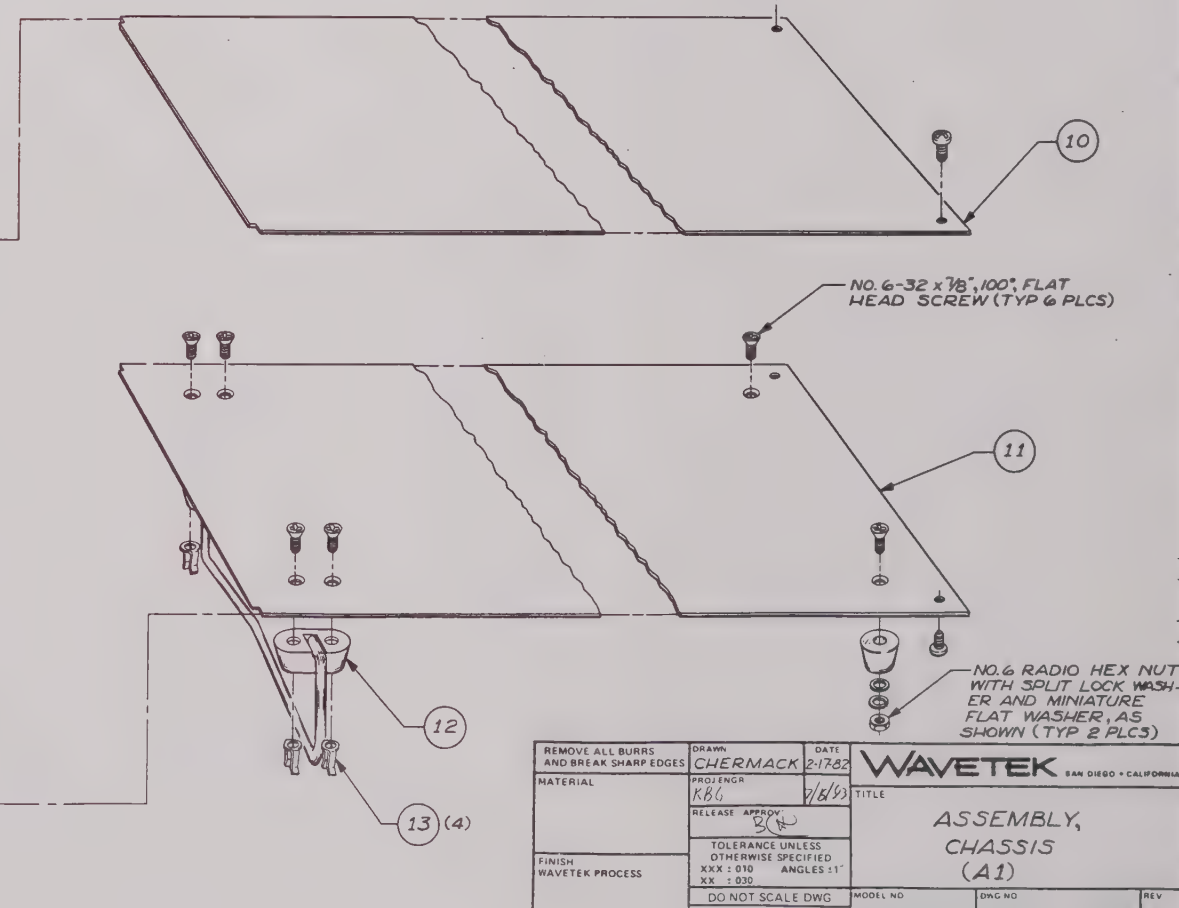
REV	ECN	BY	DATE	APP



REF NOTE (2)

WIRE LIST		
REF DES	FROM	TO
W2	A6 J3	A7 J10
W3	A6 J6	A7 J9
W5,W6,W7,W8	A7	A4 J12
W16,W17	A10	A4 J13
W14	A10 J5	A6 J17
W13	A6 J4	A10 J16
W15	A7 J14	A10 J15
W20	A7 E15	A10 J26
	A7 E16	A10 J27


SECURE COVERS TO CHASSIS WITH NO.4-40x1/4" SELF LOCKING SCREWS (TYP 2 PLCS EACH COVER)
10
NO.6-32 x 7/8", 100° FLAT HEAD SCREW (TYP 6 PLCS)
11
NO.6 RADIO HEX NUT WITH SPLIT LOCK WASHER AND MINIATURE FLAT WASHER, AS SHOWN (TYP 2 PLCS)
12
13 (4)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 2-17-82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR KBG	7/8/82	TITLE ASSEMBLY, CHASSIS (A1)
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 ANGLES ±1° XX : 030		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO 0102-00-0922 REV A
	SCALE NONE	CODE IDENT 23338	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A-3994

THIS DOCUMENT CONTAINS PROPRIETARY INFOR MATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, CHASSIS	0102-00-0922	WVTK	0102-00-0922	1
9	ASSY, SHIELD PLATE	270-0927	WVTK	1206-00-0927	1
1	ASSY, POWER ROD	270-0974	WVTK	1206-00-0974	1
2	ASSY, SIDE PLATE	270-0975	WVTK	1206-00-0975	1
4	JACK SCREW	1400-01-0530	WVTK	1400-01-0530	2
10	COVER, TOP	1400-01-3912	WVTK	1400-01-3912	1
11	COVER, BOTTOM	1400-01-3922	WVTK	1400-01-3922	1
5	TRIM, FRONT VERT, (5 1/4 IN)	MP-40282-2	BUKY	1400-01-4800	2
6	TRIM, REAR VERT, (5 1/4 IN) AIRX	MP-40281-2	BUKY	1400-01-4810	2
7	TRIM, TOP/BOTTOM (8 1/2 IN)	MP-40085-2	BUKY	1400-01-4820	2
12	BAIL ASSY W/FEET	2800-08-0018	WVTK	2800-08-0018	1
13	SPEEDNUT, SELF RETAIN	C7494-632-4	TINN	2800-09-0003	4
NONE	INSULATOR, MICA	64-21-023-106	ASHVL	3100-00-0006	5
8	RIBBON CABLE (6 INCH)	6002-00-0017	WVTK	6002-00-0017	1

WAVETEK PARTS LIST	TITLE ASSY, CHASSIS	ASSEMBLY NO. 1101-00-0922 PAGE: 1	REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST ASSY, CHASSIS
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		MODEL NO 271 / DWG NO 1101-00-0922 / REV
	DO NOT SCALE DWG		CODE IDENT 23338 / SHEET 1 OF 1
	SCALE		

BISHOP GRAPHICS INC. RECORDER NO. A27088

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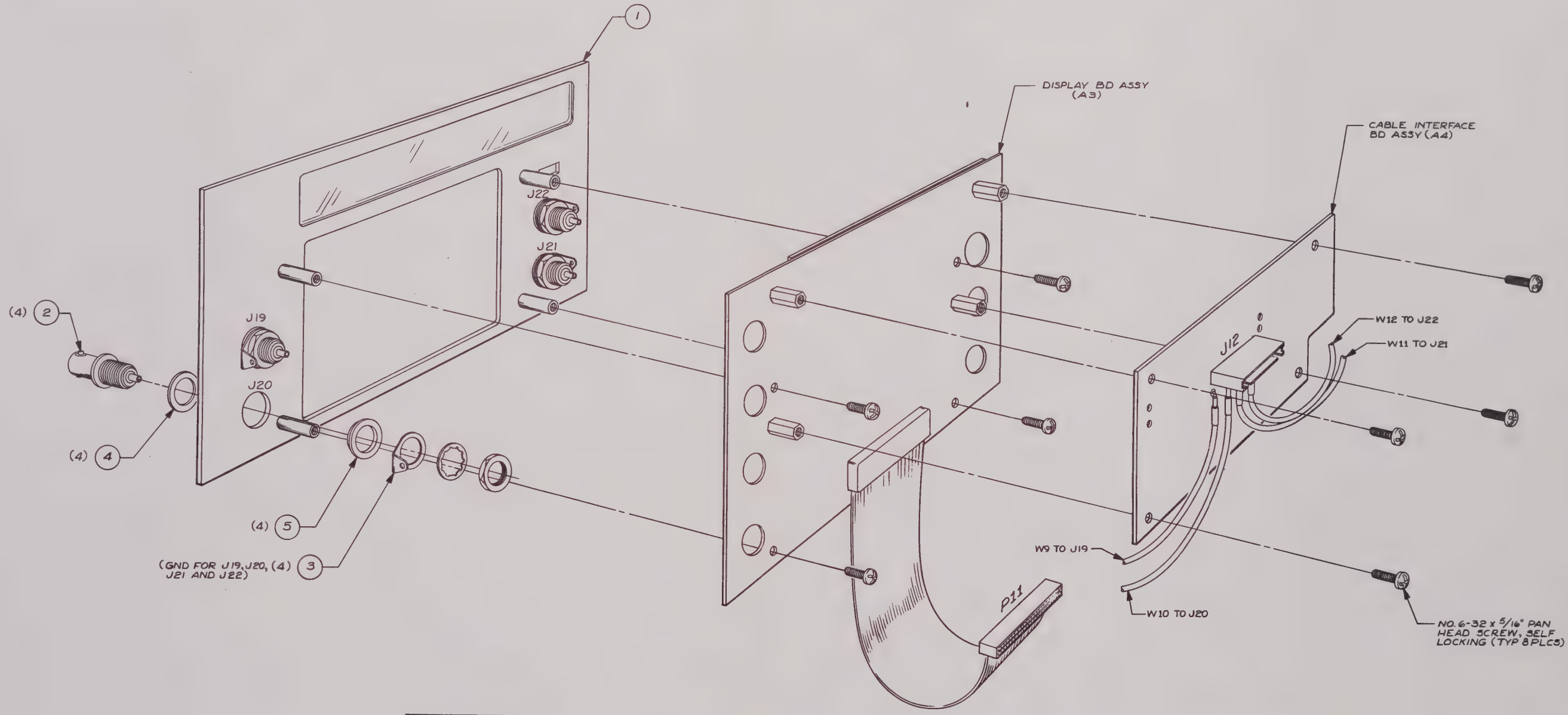
REV	ECN	BY	DATE	APP



WIRE LIST		
REF. DES.	FROM	TO
W9	A4 E1	J19
	A4 E2	J19
W10	A4 E3	J20
	A4 E4	J20
W11	A4 E5	J21
	A4 E6	J21
W12	A4 E7	J22
	A4 E8	J22

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, FRONT PANEL	0102-00-0923	WVTK	0102-00-0923	1
1	ASSY, PANEL	270-1001	WVTK	1206-00-1001	1
2	BNC CONN	KC-7946	KING	2100-01-0002	4
3	SOLDER LUG	1497	SMITH	2100-04-0012	4
5	WASHER, SHOULDER	2668	SMITH	2800-27-0004	4
4	NYLON FLAT WASHER	2264-N-385	AMTOM	2800-28-0005	4

WAVETEK PARTS LIST	TITLE ASSY, FRONT PANEL	ASSEMBLY NO. 1101-00-0999 PAGE: 1	REV

1. FOR PARTS LIST SEE 1101-00-0923 (MODEL 270)
   FOR PARTS LIST SEE 1101-00-0999 (MODEL 271)

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. CHERMACK	DATE 1-26-82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY, FRONT PANEL (A2)
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG	MODEL NO 270, 271	DWG NO 0102-00-0923 REV
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3864

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REV	ECN	BY	DATE	APP
A	# 3904	SC	8-10-83	
/	4154 CLASS III	SC	2684	

SEGMENT DRIVERS

U1 UCN4815A
U2 UCN4815A
U5A LS04
U5B LS04
R1 1K
C1 .1/50V
C2 .1/50V
C5 .1/50V

DIGIT DRIVERS

U3 UCN 4810A
U4 UCN 4810A
CR1 FD6666
CR2 FD6666
R2 1K
C3 .1/50V
C4 .1/50V
C6 .1/50V
C7 .1/50V

FILAMENT DRIVER

U8 NE555
CR3
CR4 FD6666(2)
R4 63.4K
R5 95.3K
R6 10
C11 .1/50V
C12 910PF
C13 .1/50V
C14 100/16V
C15 100/16V

VACUUM FLOURESCENT DISPLAY

V1 FG206A2

J11 DISPLAY

1 +45V
2 GND
3
4
5
6
7 +5V
8 KYBD
9 BLANK
10 DSP
11 DISP
12 GND
13 AD4
14 AD3
15 AD2
16 AD1
17 AD0
18 ADR3
19 ADR2
20 ADR1
21 ADR0
22 GND
23 DATA 7
24 DATA 6
25 DATA 5
26 DATA 4
27 DATA 3
28 DATA 2
29 DATA 1
30 DATA 0
31 GND
32 GND
33 GND
34 +15 V

C16 .1/50V
C17 .1/50V
TO GND ON INTERFACE BD (A4)
C9 100/16V

KEYBOARD

U6 74LS240
R3 10K SIP
C8 .1/50V

KEYBOARD DECODER

U7 74LS145
C10 .1/50V

4. ALL CAPACITORS ARE SHOWN IN MICRO-FARADS.
3. ALL RESISTORS ARE SHOWN IN OHMS.
2. ALL DIODES ARE FD6666.
1. REFERENCE DESIGNATORS SHOWN ARE PARTIAL, PREFIX WITH ASSEMBLY REF DES (A3).

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REORDER NO A3884

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.CHERMACK	DATE 8-17-81	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR RB6	9/15/83	TITLE SCHEMATIC, DISPLAY BOARD (A3)
FINISH WAVETEK PROCESS	RELEASE APPROV PND		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO 0103-00-0921 REV A
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

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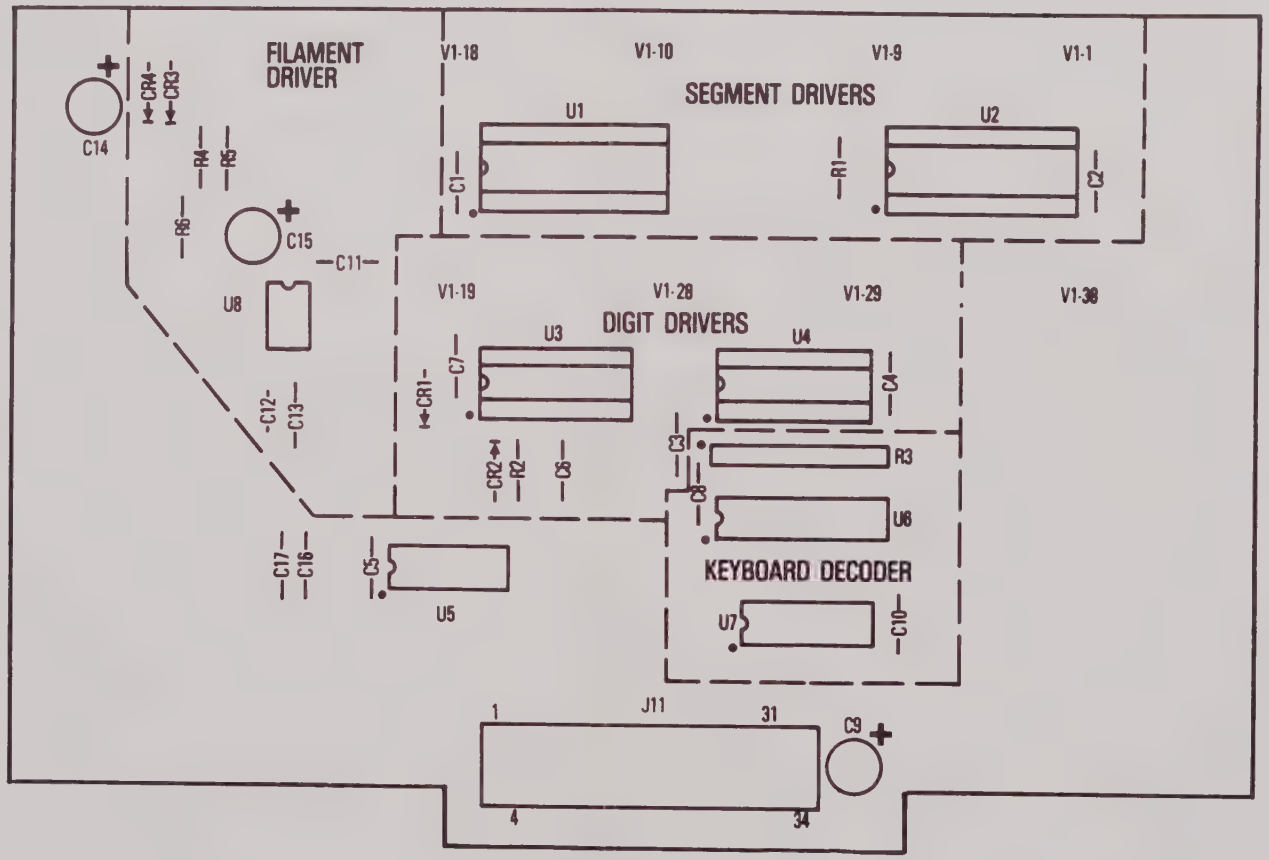

WAVETEK SAN DIEGO, CALIFORNIA	
TITLE: DISPLAY	
MODEL NO: 271	ASSY NO: 1100-00-0921 REV
CODE IDENT: 23338	SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, DISPLAY	0101-00-0921	WVTK	0101-00-0921	1
NONE	SCHEMATIC, DISPLAY	0103-00-0921	WVTK	0103-00-0921	1
NONE	ASSY, KEYBOARD	178/270-0939	WVTK	1206-00-0939	1
C1 C10 C11 C13 C16 C17 C2 C3 C4 C5 C6 C7 C8	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNO	1500-01-0405	13
C12	CAP, 910PF, 100V, 1%	DM15-911F	ARCO	1500-19-1101	1
C14 C15 C9	CAP, ELECT, 100MF, 25V RADIAL LEAD, SP .20	CRE SERIES 100/25	CAPAR	1500-31-0102	3
NONE	DISPLAY BOARD	1700-00-0921	WVTK	1700-00-0921	1
NONE	SKT, IC, 22 PIN	DILB-22P-108	BURND	2100-03-0035	2
NONE	SOCKET, 18 PIN	DIBL-18P-108	BURND	2100-03-0050	2
V1	DISPLAY, FLOUR.	FQ206A2	ITRON	2400-03-0009	1
NONE	STANDOFF, SWAGE .300 H, .250 HEX 6-32, .062 MAT'L	1531B-1/2-11	USECO	2800-02-0003	4
R1 R2	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	2
R6	RES, MF, 1/8W, 1%, 10	RN55D-10R0F	TRW	4701-03-1009	1
R4	RES, MF, 1/8W, 1%, 63.4K	RN55D-6342F	TRW	4701-03-6342	1
R5	RES, MF, 1/8W, 1%, 95.3K	RN55D-9532F	TRW	4701-03-9532	1

WAVETEK PARTS LIST	TITLE PCA, DISPLAY	ASSEMBLY NO. 1100-00-0921 PAGE: 1	REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R3	RES MODULE, 10K	4310R-101-103	BOURN	4770-00-0008	1
CR1 CR2 CR3 CR4	DIODE	1N4148	FAIR	4807-02-6666	4
W4	ASSY, RIBBON CABLE	922522-34-02-4.5	A/P	6002-00-0009	1
U8	IC	NE555V	SIG	7000-05-5500	1
U3 U4	IC, DISPLAY DRIVER	UCN4810A	SPRAG	8000-48-1000	2
U1 U2	IC, DISPLAY DRIVER	UCN4815A	SPRAG	8000-48-1500	2
U5	IC	74LS04	TI	8000-74-0410	1
U7	IC	74LS145	SIG	8007-41-4510	1
U6	IC	74LS240	TI	8007-42-4010	1

WAVETEK PARTS LIST	TITLE PCA, DISPLAY	ASSEMBLY NO. 1100-00-0921 PAGE: 2	REV A

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA DISPLAY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 271	DWG NO 1100-00-0921 REV A
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

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REV	ECN	BY	DATE	APP
A	#3904	SC	7-27-84	
/	4144 CLASS III	SC	2-7-84	

VCG & TRIGGER LEVEL

VCG COMPENSATION
VCG AMPLIFIER
CURRENT SOURCES
TRIGGER LEVEL AMPLIFIER
TRIGGER COMPARATOR & SLOPE LOGIC
MODE LOGIC

TRIGGER CIRCUIT

9. * NOMINAL VALUE CALLED OUT ON PARTS LIST.
6. MATCH SET RESISTORS (3) P/N 4789-00-0043 (REF R113, R114, R115)
5. MATCHED SET CAPACITORS (3) P/N 1509-80-0008 (REF C50, C52, C54)
4. MATCHED PAIR FD777 DIODES P/N 4898-00-0004 (REF CR8, CR7)
3. MATCHED SET .1% RESISTORS (4) P/N 4701-02-7500 (REF R194, R198, R189, R192)
4. ALL CAPACITORS ARE IN MICRO-FARADS.
3. ALL DIODES ARE FD6666
2. ALL RESISTORS ARE IN OHMS.
1. REFERENCE DESIGNATORS SHOWN ARE PARTIAL, PREFIX WITH ASSEMBLY REF DES (A7)

NOTE UNLESS OTHERWISE SPECIFIED

LAST USED	NOT USED
R303	R143, R144
C126	
CR66	
U20	
Q41	
K3	
E16	
TP1	

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. THOMPSON	DATE 11-23-83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR PBL	7/15/85	TITLE: SCHEMATIC FUNCTION GENERATOR BOARD (A7)
	RELEASE APPROV EW		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		
	SCALE	MODEL NO 270, 271, 273, 278	DWG NO 0103-00-0920 REV A
		CODE IDENT 23338	SHEET 1 OF 4

7-13

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REV	ECN	BY	DATE	APP

FREQUENCY COMPENSATION

HIGH FREQUENCY COMPENSATION

C15 .1 · +5V · +15VR · C56 .1 · R44 243K · R53 4.99K · C18 .1 · R55 4.99K · R56 2K · C16 10PF · R38 10K · VCV · R39 15K · C19 .1 · DG211 U8C · R42 1K CW · R45 2K · 9.99MHz ADJ · FR7 · DG211 U7C · TL084 · DG211 U8B · R40 10K · R43 20K · R46 20K CW · 999KHz ADJ · FR6 · C20 10PF · CR15 IN751A · Q2 2N5462 · R50 4.99K · U7B · TL084 · +COMP · -COMP · R54 10K · DG211 U8A · R41 301K · R47 499K · FR5 · CR16 IN751A · Q3 2N5485 · R51 4.99K · U7A · TL084 · C21 10PF · R52 10K · R57 10K · C17 .1 · DG211 U8A · DCA · R59 1.78K · TL084 · U7D · C23 .1 · DG211 U8B · R48 10M · R49 10M · C22 5PF · C58 .1 · R58 4.99K · R60 500 CW · TRI BAL · -15VR

GENERATOR LOOP

CURRENT SWITCH · SWITCH BUFFER · COMPARATOR · SQUARE BUFFER · TRIANGLE BUFFER

+5V · +15VR

R61 6.98K · +I · Q4 2N5462 · R62 15.8K · C25 .1 · R65 4.7, 1/2W · C28 · R72 6.19K · CR24 HP2811 · R76 2K · R77 499 · R78 2K · CR31 HP2811 · R84 1.78K · R92 150 · C33 .001 · CR66 IN959B · C34 · C57 .1

Q6 2N3563 · R66 100 · Q8 2N5771 · R74 33.2 · R79 33.2 · Q12 2N5771 · R85 100 · Q13 2N3563

CR17 · CR18 · FD777 (4) · CR19 · CR20 · R67 4.7, 1/2W · R68 4.7, 1/2W · CR22 IN4148 · R70 10 · R73 332 · CR23 IN4148 · Q7 2N5771 · R69 100 · CR29 FD777 · CR30 FD777 · R86 392 · CR32 IN4148 · R93 4.7 1/2W · R88 10 · R94 4.7 1/2W · C35 5PF · C36 5PF · CR33 IN4148 · Q14 2N5771 · R89 100 · SQB · SQS · TRITST · TRB · R100 221 · R101 221 · R102 10K · R103 1K

CR25 · CR26 · IN4148 (4) · CR27 · CR28 · Q9 2N3563 · Q11 2N3563 · R87 332 · R90* · CR34 IN4740A · CR21 IN4740A · R71 2.49K · R75 332 · Q15 2N5485 · Q16 2N3563 · Q17 2N3904 · C37 .1 · R98 1K · R99 10K CW · R104 10K · NODE DC

Q5 2N5485 · C26 .1 · R64 6.98K · -I · C27 5PF · C29 .1 · R80 100 · Q10 2N3563 · R81 1.1K · R82 1K · C30 .1 · C31 .1 · R83 2.49K · R91 4.99K · C32 .1 · R95 10K · R97 10

R63 33.2 · -15VR · -15V · R302 10K · DCCOMP

TRIANGLE BUFFER OUTPUT
DC COMPENSATION
TRIANGLE NODE

TRN — DC AMPLIFIER

1 MHz ADJ · C43 3.5-13 PF · C44 * · C45 7-35 PF · C46 56PF SM · C47 820 PF SM · 100 KHz ADJ · C50 .01 ⚠7 · C52 .1 ⚠7 · C54 1.0 ⚠7

CAPACITANCE MULTIPLIER

+15VR · +5V · R119 100 · C41 .1 · DG211 U10C · R112 200 · R111 825 CW · 99.9 Hz ADJ · FR2 · R113 10K ⚠8 · DG211 U10B · R105 20K CW · R106 49.9K · 999 Hz ADJ · FR1 · R114 100K ⚠8 · C38 .1 · C42 .01 · TL083 U9A · R109 100 · C40 MYLAR · R110 10 · FRØ · R115 1M ⚠8 · R107 10K · R108 10K · C39 .1 · TL083 U9B · R118 1.21K · DG211 U8D · R116 10K · R117 100K CW · CPM · 1Hz SYM · U10D DG211 · -15VR

FREQUENCY RANGE SWITCHES

+5V · CR35 IN4148 · Q18 2N3906 · R126 2.21K FR6 · C48 .001 · Q19 2N3906 · R130 2.21K FR5 · C51 .001 · Q20 2N3906 · R134 2.21K FR4 · C53 .001 · Q21 2N3906 · R138 2.21K FR3 · C55 .001 · R120 4.64K · R124 90.9 · R128 90.9 · R132 90.9 · R136 90.9 · CR36 IN5282 · CR38 IN5282 · CR40 IN5282 · CR42 IN5282 · R121 7.5K · R123 10M · CR37 IN5282 · R125 20K · R127 10M · CR39 IN5282 · R129 20K · R131 10M · CR41 IN5282 · R133 20K · R135 10M · CR43 IN5282 · R137 20K · R122 7.5K · C49 .1 · -15V

⚠8 SEE PAGE 1
⚠7 SEE PAGE 1
NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. THOMPSON	DATE 11-23-81	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR	7/8/82	TITLE: SCHEMATIC FUNCTION GENERATOR BOARD (A7)
FINISH WAVETEK PROCESS	RELEASE APPROVAL		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		MODEL NO 270, 271, 273, 278 · DWG NO 0103-00-0920 · REV A
	DO NOT SCALE DWG · SCALE		CODE IDENT 23338 · SHEET 2 OF 4

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-2864

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REV	ECN	BY	DATE	APP

J9
LOGIC

FRQ	1	FRQ
AMP	2	AMP
OST	3	OST
TRL	4	TRL
ANLØ	5	$\overline{FRØ}$
ANL1	6	$\overline{FR1}$
ANL2	7	$\overline{FR2}$
ANL3	8	$\overline{FR3}$
ANL4	9	$\overline{FR4}$
ANL5	10	$\overline{FR5}$
ANL6	11	$\overline{FR6}$
ANL7	12	$\overline{FR7}$
ANL8	13	OAØ
ANL9	14	
ANL10	15	OA2
ANL11	16	MCØ
ANL12	17	MC1
ANL13	18	$\overline{DCA}$
ANL14	19	$\overline{OVR}$
ANL15	20	$\overline{CPM}$
ANL16	21	-TR
ANL17	22	+TR
ANL18	23	EXW
ANL19	24	$\overline{SQR}$
ANL20	25	SQR
ANL21	26	$\overline{SIN}$
ANL22	27	$\overline{TRI}$
ANL23	28	$\overline{RCT}$
ANL24	29	$\overline{PLS}$
ANL25	30	PLS
ANL26	31	
ANL27	32	
PORTIØ	33	OAP
PORTI1	34	FUB

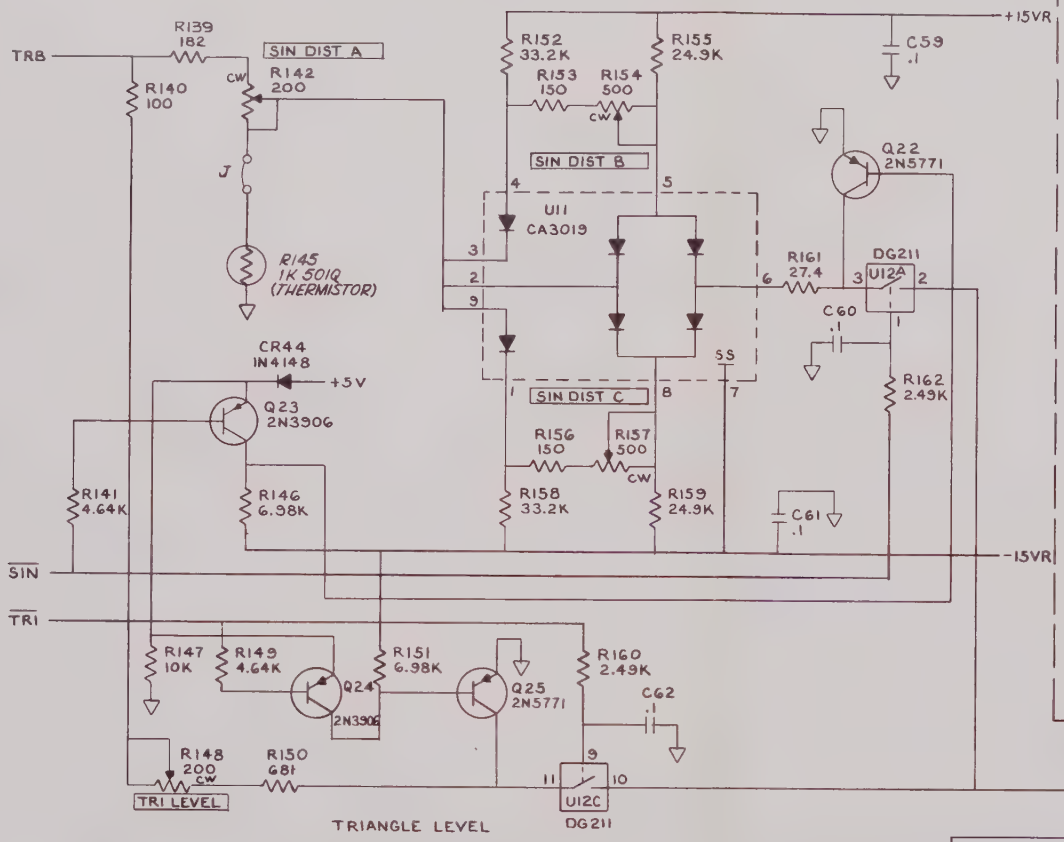
J14
AUX

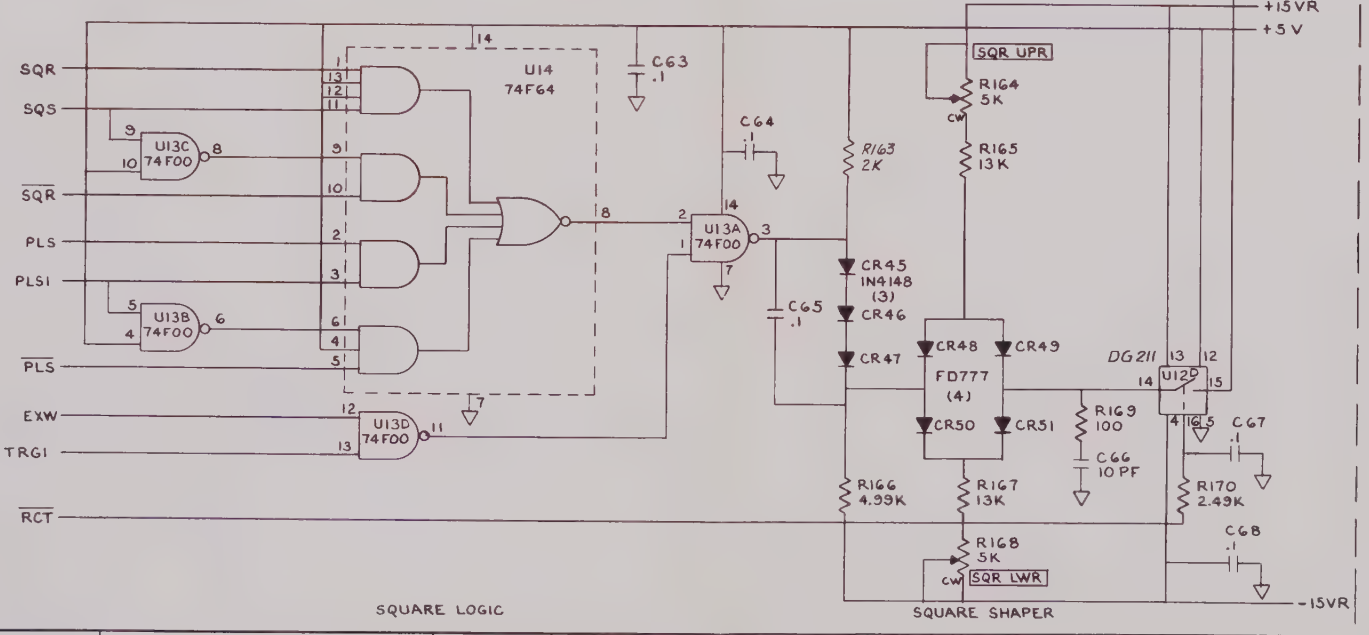
GND	1	
VCG1	2	VCG1
GND	3	
VCGO	4	VCGO
GND	5	
GND	6	
TRG1	7	TRG1
GND	8	
TRGO	9	TRGO
GND	10	
PLS1	11	PLS1
GND	12	
SQS	13	SQS
GND	14	

NOTE UNLESS OTHERWISE SPECIFIED

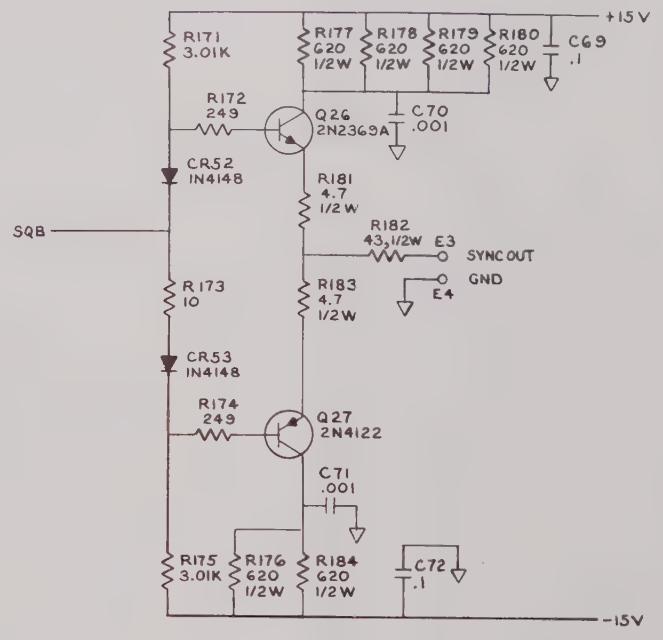
FUNCTION SELECT

SINE CONVERTER





SYNC DRIVER



J23
TEST

PATEST	1	PATEST
+15V	R185 2	+15VT
-15V	R186 3	-15VT
+5V	R187 100(3) 4	GND
	5	+5VT
	6	GND
TRITST	7	TRITST
	8	GND
DCCOMP	9	DCCOMP
	10	GND
VCGTST	11	VCGTST
	12	GND
AMPLDC	13	AMPLDC
	14	GND

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.THOMPSON	DATE 11-23-81	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR RBG	1/5/83	TITLE SCHEMATIC FUNCTION GENERATOR BOARD (A7)
FINISH WAVETEK PROCESS	RELEASE APPROV BJH		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 270, 271 273, 278
	SCALE		DWG NO 0103-00-0920 REV A
			CODE IDENT 23338 SHEET 3 OF 4

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3514

7-15

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REV	ECN	BY	DATE	APP

PREAMPLIFIER

OUTPUT AMPLIFIER

J10 POWER: GND 1, GND 2, +5V 3, GND 4, -15V 5, -15V 6, GND 7, GND 8, +15V 9, +15V 10

C73 .1 · C74 .1 · C75 .1 · +15V

R190 5.76K · R191 1K · C77 .1 · Q28 2N5771 · R188 10K · C76 .1 · +5V · C123 22/15

R196 5.76K · R197 1K · C78 .1 · R96 200 · Q29 2N5771 · R193 10K · C79 .1

U15C CA3083 · C80 5PF · C81 5PF · R192 750,.1% (5) · R194 750,.1% (5) · R189 750,.1% (5) · U15B CA3083 · R195 2.49K

U15D CA3083 · C82 1.5 PF · R198 750,.1% (5) · CR54 IN751A · U15A CA3083 · R199 750

C83 .1 · C88 .1 · C95 .1 · C103 .1

R201 1K · R202 1K · U16B CA3096 · C86 150 PF · R203 221

U16A CA3096 · R200 150 · R205 42.2 · OFFSET ADJ · R207 150 · R208 100 CW · R204 10K · PATEST · R206 3.32K · R209 464 · C87 .001

R210 150 · R211 100 · C89 .1 · R212 2K · R213 24.9K · C90 .1 · R214 2K · C92 .1 · R215 100 · C91 .1

Q30 2N3563 · R216 4.99K · C93 .1 · Q31 2N5771 · C122 3.5-13 · R217 909 · C94 10PF · O.A. ROLL OFF

R218 51.1 · C96 .1 · R221 21.5 · Q32 2N2905A · CR55 IN4148 · R219 10 · CR56 IN4148 · Q33 2N2219A · C98 .1 · R225 21.5 · R220 100 · 2800-11-0008 HEAT SINK (2)

R222 100 · R223 90.9 · R224 750 · C97 7-35PF · O.A. PEAKING · Q34 · Q35 2N2219A (2) · Q36 · Q37 2N2905A (2)

R226 10 · R230 10 · C99 .1 · C100 22/15 · R227 10 · R231 10 · R228 10 · R232 10 · C101 .1 · C102 22/15 · R229 10 · R233 10 · C84 .1 · C85 .1

+15V · CR57 IN5282 · 2800-11-0012 HEAT SINKS (4) · CR58 IN5282 · -15V

OST · R234 10K · R235 4.99K · R236 4.99K · C104 .1 · U17C TL084 · R239 27.4K · R237 2K CW · R238 1.62K · -15VR · OFFSET ZERO · OFFSET

MODEL 275 ONLY

E15 ARB IN · E16 GND · R300 TRIM · C105 .1 · R240 4.64K · HI AMPL ADJ · R242 2K CW · C106 .1 · R241 1K · MULT DC BAL CW · R243 6.81K · XY1

U18 CA3054 · R244 100 · R247 100 · R248 1.1K · R245 1.1K · R246 1.1K · CR59 IN4148 · CR60 IN823A · R249 1.21K · C110 .1

R251 100K CW · LO AMPL ADJ · -15VR · C107 .1 · R254 499K · R256 1K · R257 1K · U17D TLO84 · R258 4.99K · C108 .1 · AMPLDC · R264 10K · MULT. DIST.

U17A TL084 · R252 27.4K CW · R253 27.4 · R255 20K · R259 27.4 · R260 4.99K · C109 22PF · R265 10K

U19 CA3054 · R250 100 · R261 100 · CR61 IN751A · TL084 U17B · R262 1.21K · R263 2K · CR62 IN4148 · C111 .1 · C112 .1 · R267 7.5K · R266 2.49K · C113 .1 · -15VR · AMP

XY MULTIPLIER

5. SEE PAGE 1 NOTE UNLESS OTHERWISE SPECIFIED

XY MULTIPLIER & OFFSET

+5V · R277 4.99K · R278 15K · FUB · FUSE SENSE · C117 .1 · C118 .1 · U20D LM339 · R285 100K · R286 1M · R287 100K · R288 1M · F1 FUSE P/N 1200-00-0977 · +15V · -15V

C114 10 PF · R270 1M · R276 1M · R279 4.99K · +5V

R268 CR63 499K IN4148 · R269 CR64 499K IN4148 · U20B LM339 · R271 78.7K · R274 78.7K · R272 78.7K · R275 78.7K · U20C LM339 · R273 1M · -15V · CR65 IN4148 · C116 .1

OAP · OAØ · OA2 · R280 2.21K · Q38 2N3638A · Q39 2N3904 · R281 4.99K · R282 3.01K · Q40 2N3904 · R283 4.99K · Q41 2N3904 · R284 3.01K · C119 .1 · C120 .1 · C121 .1

K1 · K2 · K3 · RA3157-1051 (3) · OUTPUT ATTENUATOR

R289 1.96K(4) · R290 · R291 · R292 · R295 20 CW · ATTEN ADJ · R293 100,1W · R294 100,1W · R296 10 · R297 12.4 · R298 1M · R299 1M · E1 FUNC OUT · E2 GND

OUTPUT PROTECTION

C115 10 PF · OVERVOLTAGE SENSE

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. THOMPSON	DATE 11-23-84	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR RBS		TITLE SCHEMATIC FUNCTION GENERATOR BOARD (A7)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 270, 271, 273, 278 · DWG NO 0103-00-0920 · REV A
	SCALE		CODE IDENT 23338 · SHEET 4 OF 4

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3884

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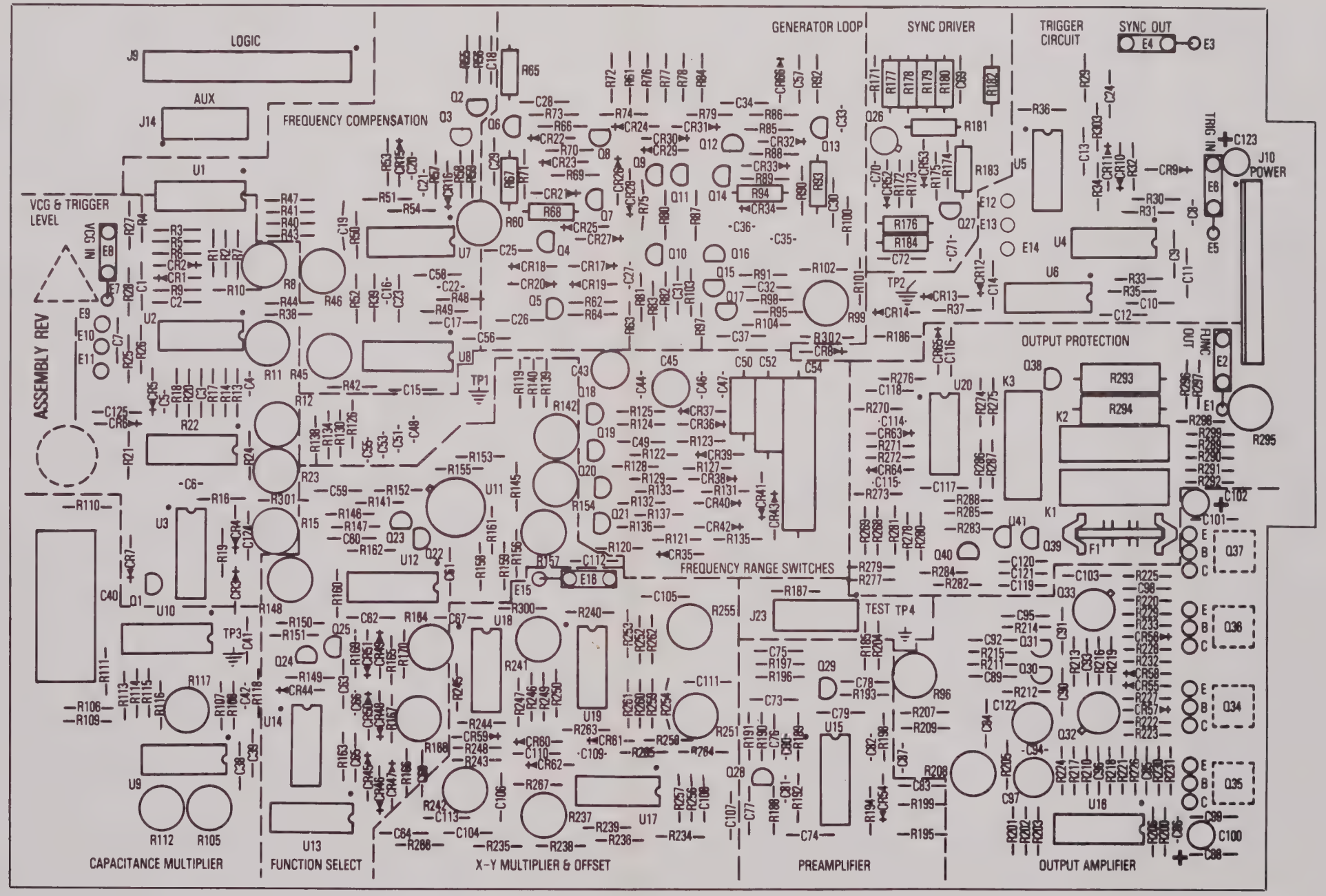

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: FUNCTION GENERATOR ASSEMBLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES 1 XX .030		
	DO NOT SCALE DWG		MODEL NO 271 · DWG NO 1100-00-0920 · REV
	SCALE		CODE IDENT 23338 · SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, FUNCTION GENERATOR	0101-00-0920	WVTK	0101-00-0920	1
NONE	SCHEMATIC, FUNCTION GENERATOR	0103-00-0920	WVTK	0103-00-0920	1
F1	PCA, OUTPUT FUSE BD	1200-00-0977	WVTK	1200-00-0977	1
NONE	ASSY, XSISTOR MNTG ANGLE	270-1009	WVTK	1206-00-1009	1
C22 C27 C35 C36 C8 C80 C81	CAP, CER, 3PF, 1KV	DD-030	CRL	1500-00-5011	7
C114 C115 C16 C20 C21 C66 C94	CAP, CER, 10PF, 1KV	DD-100	CRL	1500-01-0011	7
C4 C5	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	2
C33 C48 C51 C53 C55 C70 C71 C87	CAP, CER, .001MF, 1KV	DD-102	CRL	1500-01-0211	8
C42	CAP, CER, MN, .01MF, 50V	CAC02Z5U103Z100A	CORNG	1500-01-0310	1
C1 C10 C101 C103 C104 C105 C106 C107 C108 C11 C110 C111 C112 C113 C116 C117 C118 C119 C12 C120 C121 C124 C125 C13 C14 C15 C17 C18 C19 C2 C23 C24 C25 C26 C28 C29 C3 C30 C31 C32 C34 C37 C38 C39 C41 C49	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	82

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — PAGE: 1 — REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	CAP SET, POLYC MIXED MATCHED SET	180-501	WVTK	1509-80-0008	1
C50	CAP, POLYC, .01MF, 100V PART OF 1509-80-0008 QTY(1)				
C52	CAP, POLYC, .1MF, 100V PART OF 1509-80-0008 QTY(1)				
C54	CAP, POLYC, 1MF, 100V PART OF 1509-80-0008 QTY(1)				
NONE	FUNCTION GENERATOR	1700-00-0920	WVTK	1700-00-0920	1
J10	CONN HEADER	09-60-1101	MOLEX	2100-02-0088	1
J14	CONN, HOUSING, 14 PIN WITH POLARIZING TABS	2100-02-0136	WVTK	2100-02-0136	1
J9	CONN, HOUSING, 34 PIN WITH POLARIZING TABS	2100-02-0138	WVTK	2100-02-0138	1
NONE	TERM	2000B1	USECO	2100-05-0009	12
TP1 TP2 TP3 TP4	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	4
J23	HEADER, 14 PIN, 2X7	CA-D14RSP100-230-090	CA	2100-05-0053	1
NONE	SPACER, HINGED .750H, .250D 6-32 THD	LT3021	LYNTR	2800-03-0009	2

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — PAGE: 3 — REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R237 R242 R43	POT, TRIM, 2K	91AR2K	BECK	4600-02-0201	3
R105 R255 R46	POT, TRIM, 20K	91AR20K	BECK	4600-02-0301	3
R154 R157 R60	POT, TRIM, 500	91AR500	BECK	4600-05-0104	3
R164 R168	POT, TRIM, 5K	91AR5K	BECK	4600-05-0203	2
R182	RES, C, 1/2W, 5%, 43	RC20GF-430	STKPL	4700-25-0430	1
R181 R183 R65 R67 R68 R93 R94	RES, C, 1/2W, 5%, 4.7	RC20GF-4R7	STKPL	4700-25-0479	7
R176 R177 R178 R179 R180 R184	RES, C, 1/2W, 5%, 620	RC20GF621	STKPL	4700-25-6200	6
R189 R192 R194 R198	RES, MF, 1/8W, .1%, 750	RN55E-7500B	MEPCO	4701-02-7500	4
R109 R119 R140 R169 R185 R186 R187 R211 R215 R220 R222 R244 R247 R250 R261 R66 R69 R80 R85 R89	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	20
R103 R14 R17 R18 R191 R197 R20 R201 R202 R256 R257 R42 R82 R98	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	14
R102 R104 R107 R108 R116 R147 R188 R193 R204 R234 R264 R265 R301 R302 R38 R40 R52 R54 R57 R6 R95	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	21

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — PAGE: 5 — REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C67 C68 C69 C7 C72 C73 C74 C75 C76 C77 C78 C79 C83 C84 C85 C88 C89 C9 C90 C91 C92 C93 C95 C96 C98 C99					
C86	CAP, CER, 150PF, 1KV	DD-151	CRL	1500-01-5111	1
C82	CAP, CER, 1.5PF, 1KV	10TCC-V15	SPRAG	1500-01-5507	1
C109	CAP, CER, 22PF, 1KV	DD-220	CRL	1500-02-2011	1
C6	CAP, CER, 220PF, 1KV	DD-221	CRL	1500-02-2111	1
C44T	CAP, CER, 33PF, 1KV	DD-330	CRL	1500-03-3011	1
C46	CAP, MICA, 56PF, 500V	DM15-560J	ARCO	1500-15-6000	1
C47	CAP, MICA, 820PF, 300V	DM15-821F	ARCO	1500-18-2101	1
C40	CAP, MYLR, 2MF, 200V	2MFW205K	AMRAD	1500-42-0504	1
C122 C43	VARI, 3.5-13PF, 250V	7S-TRIKO-02 3.5/13PF	TRIKO	1500-51-3000	2
C45 C97	VARI, 7-35PF, 250V	7S-TRIKO-02 7/35 PF	TRIKO	1500-53-5000	2
C100 C102 C123	CAP, TANT, 22MF, 15V	196D226X9015KA1	SPRAG	1500-72-2601	3

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — PAGE: 2 — REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SPACER .750H, .250 HEX 6-32 THRU	2323	SMITH	2800-03-0010	2
NONE	SPACER, SWAGE .562H, .250 DIA .150DIA THRU, .062MTL	6310-9/16-2C	LNTRN	2800-04-0017	3
NONE	HEAT SINK	207	WAKE	2800-11-0001	2
NONE	TRANSIPAD	10160	METRS	2800-11-0004	2
NONE	JUMPER	461-2871-01-03-10	CAMB	3000-00-0034	2
E10 E11 E12 E13 E14 E9	PINS, JUMPER	450-3704-01-03	CAMB	3000-00-0035	6
NONE	DIGI-CLIP	MC-20	CMPCP	3000-00-0093	4
NONE	DIGI-GUIDE	MC-10-1/2	CMPCP	3000-00-0094	2
K1 K2 K3	RELAY, REED, FORM-A	RA3019-1051	ETROL	4500-00-0007	3
R208 R23	POT, TRIM, 100	91AR100	BECK	4600-01-0103	2
R241 R9	POT, TRIM, 1K	91AR1K	BECK	4600-01-0209	2
R99	POT, TRIM, 10K	91AR10K	BECK	4600-01-0315	1
R11 R117 R12 R15 R231	POT, TRIM, 100K	91AR100K	BECK	4600-01-0402	5
R295	POT, TRIM, 20	91AR20	BECK	4600-02-0000	1
R112 R142 R148 R96	POT, TRIM, 200	91AR200	BECK	4600-02-0101	4

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — PAGE: 4 — REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R285 R287 R33 R35	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	4
R10 R16 R270 R273 R276 R286 R288 R298 R299 R3	RES, MF, 1/8W, 1%, 1M	RN55D-1004F	TRW	4701-03-1004	10
R110 R173 R219 R226 R227 R228 R229 R230 R231 R232 R233 R296 R70 R88 R97	RES, MF, 1/8W, 1%, 10	RN55D-10R0F	TRW	4701-03-1009	15
R245 R246 R248 R81	RES, MF, 1/8W, 1%, 1.1K	RN55D-1101F	TRW	4701-03-1101	4
R118 R249 R262	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	3
R297	RES, MF, 1/8W, 1%, 12.4	RN55D-12R4F	TRW	4701-03-1249	1
R165 R167	RES, MF, 1/8W, 1%, 13K	RN55D-1302F	TRW	4701-03-1302	2
R153 R156 R200 R207 R210 R92	RES, MF, 1/8W, 1%, 150	RN55D-1500F	TRW	4701-03-1500	6
R278 R39	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	2
R1 R2	RES, MF, 1/8W, 1%, 150K	RN55D-1503F	TRW	4701-03-1503	2
R62	RES, MF, 1/8W, 1%, 15.8K	RN55D-1582F	TRW	4701-03-1582	1
R238	RES, MF, 1/8W, 1%, 1.62K	RN55D-1621F	TRW	4701-03-1621	1
R59 R84	RES, MF, 1/8W, 1%, 1.78K	RN55D-1781F	TRW	4701-03-1781	2
R139	RES, MF, 1/8W, 1%, 182	RN55D-1820F	TRW	4701-03-1820	1

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — PAGE: 6 — REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, FUNCTION GENERATOR
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		MODEL NO 271 — DWG NO 1100-00-0920 — REV
	DO NOT SCALE DWG		CODE IDENT 23338 — SHEET 1 OF 2
	SCALE		

BISHOP GRAPHICS, INC/EXPRESS REVISED NO. A2/088

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R289 R290 R291 R292	RES, MF, 1/8W, 1%, 1.96K	RN55D-1961F	TRW	4701-03-1961	4
R163 R212 R214 R263 R56 R76 R78	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	7
R125 R129 R133 R137 R26 R43	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	6
R221 R225	RES, MF, 1/8W, 1%, 21.5	RN55D-21R5F	TRW	4701-03-2159	2
R100 R101 R203	RES, MF, 1/8W, 1%, 221	RN55D-2210F	TRW	4701-03-2210	3
R126 R130 R134 R138 R290	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	5
R24	RES, MF, 1/8W, 1%, 23.7K	RN55D-2372F	TRW	4701-03-2372	1
R44	RES, MF, 1/8W, 1%, 243K	RN55D-2433F	TRW	4701-03-2433	1
R172 R174	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	2
R160 R162 R170 R195 R266 R303 R32 R34 R36 R71 R83 R9	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	12
R155 R159 R213 R30	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	4
R239 R252	RES, MF, 1/8W, 1%, 27.4K	RN55D-2742F	TRW	4701-03-2742	2
R161 R253 R259	RES, MF, 1/8W, 1%, 27.4	RN55D-27R4F	TRW	4701-03-2749	3
R171 R175 R282 R284	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	4
R25	RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	1

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — PAGE: 7 — REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R218	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	1
R190 R196	RES, MF, 1/8W, 1%, 5.76K	RN55D-5761F	TRW	4701-03-5761	2
R72 R90T	RES, MF, 1/8W, 1%, 6.19K	RN55D-6191F	TRW	4701-03-6191	2
R150	RES, MF, 1/8W, 1%, 681	RN55D-6810F	TRW	4701-03-6810	1
R243	RES, MF, 1/8W, 1%, 6.81K	RN55D-6811F	TRW	4701-03-6811	1
R146 R151 R61 R64	RES, MF, 1/8W, 1%, 6.98K	RN55D-6981F	TRW	4701-03-6981	4
R199 R224	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	2
R121 R122 R267 R31	RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	4
R271 R272 R274 R275	RES, MF, 1/8W, 1%, 78.7K	RN55D-7872F	TRW	4701-03-7872	4
R111	RES, MF, 1/8W, 1%, 825	RN55D-8250F	TRW	4701-03-8250	1
R37	RES, MF, 1/8W, 1%, 8.25K	RN55D-8251F	TRW	4701-03-8251	1
R217	RES, MF, 1/8W, 1%, 909	RN55D-9090F	TRW	4701-03-9090	1
R124 R128 R132 R136 R223	RES, MF, 1/8W, 1%, 90.9	RN55D-90R9F	TRW	4701-03-9099	5
R293 R294	RES, MF, 1W, 1%, 100	RN70D-1000F	TRW	4701-33-1000	2
R22	RES MODULE	4116R-001-102	BOURN	4770-00-0019	1

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — PAGE: 9 — REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR14 CR2 CR22 CR23 CR25 CR26 CR27 CR28 CR3 CR32 CR33 CR35 CR44 CR45 CR46 CR47 CR5 CR52 CR53 CR55 CR56 CR59 CR62 CR63 CR64 CR65 CR9					
CR24 CR31	DIODE	5082-2811	HP	4809-02-2811	2
CR7 CR8	DIODE, M/PR, FD-777 QTY: 2: 4807-02-0777	164-501-93	WVTK	4898-00-0004	1
Q33 Q34 Q35	TRANS	2N2219A	NSC	4901-02-2191	3
Q26	TRANS	2N2369A	MOT	4901-02-3691	1
Q32 Q36 Q37	TRANS	2N2905A	NSC	4901-02-9051	3
Q10 Q11 Q13 Q16 Q30 Q6 Q9	TRANS	2N3563	FAIR	4901-03-5630	7
Q38	TRANS	2N3638A	CARTR	4901-03-6381	1
Q1	TRANS	2N3903	NSC	4901-03-9030	1
Q17 Q39 Q40 Q41	TRANS	2N3904	FAIR	4901-03-9040	4
Q18 Q19 Q20 Q21 Q23 Q24	TRANS	2N3906	FAIR	4901-03-9060	6
Q27	TRANS	2N4122	NSC	4901-04-1220	1
Q2 Q4	TRANS	2N5462	MOT	4901-05-4620	2

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — PAGE: 11 — REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R41	RES, MF, 1/8W, 1%, 301K	RN55D-3013F	TRW	4701-03-3013	1
R73 R75 R87	RES, MF, 1/8W, 1%, 332	RN55D-3320F	TRW	4701-03-3320	3
R206	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	1
R152 R158	RES, MF, 1/8W, 1%, 33.2K	RN55D-3322F	TRW	4701-03-3322	2
R63 R74 R79	RES, MF, 1/8W, 1%, 33.2	RN55D-33R2F	TRW	4701-03-3329	3
R7	RES, MF, 1/8W, 1%, 3.57K	RN55D-3571F	TRW	4701-03-3571	1
R86	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	1
R205	RES, MF, 1/8W, 1%, 42.2	RN55D-42R2F	TRW	4701-03-4229	1
R209	RES, MF, 1/8W, 1%, 464	RN55D-4640F	TRW	4701-03-4640	1
R120 R141 R149 R240	RES, MF, 1/8W, 1%, 4.64K	RN55D-4641F	TRW	4701-03-4641	4
R77	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	1
R166 R19 R21 R216 R235 R236 R258 R260 R27 R277 R279 R28 R281 R283 R29 R4 R5 R50 R51 R53 R55 R58 R91	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	23
R106	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	1
R13 R254 R268 R269 R47	RES, MF, 1/8W, 1%, 499K	RN55D-4993F	TRW	4701-03-4993	5

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — PAGE: 8 — REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R113	RES, MF, MIXED SET	4789-00-0043	WVTK	4789-00-0043	1
	RES, MF, 1/8W, 1%, 10K PART OF 4789-00-0043 QTY(1)				
R114	RES, MF, 1/8W, 1%, 100K PART OF 4789-00-0043 QTY(1)				
R115	RES, MF, 1/4W, 1%, 1M PART OF 4789-00-0043 QTY(1)				
R123 R127 R131 R135 R48 R49	RES, MF, 1/4W, 1%, 10M	CC1005F	AB	4799-00-0056	6
CR11 CR15 CR16 CR54 CR61	DIODE	1N751A	FAIR	4801-01-0751	5
CR60	DIODE, ZENER 6.2V	1N823A	MOT	4801-01-0823	1
CR4 CR6 CR66	DIODE	1N959	SIEM	4801-01-0959	3
CR21 CR34	DIODE	1N4740A	MOT	4801-01-4740	2
CR36 CR37 CR38 CR39 CR40 CR41 CR42 CR43 CR57 CR58	DIODE	1N5282	FAIR	4801-01-5282	10
CR17 CR18 CR19 CR20 CR29 CR30 CR48 CR49 CR50 CR51	DIODE	FD777	FAIR	4807-02-0777	10
CR1 CR10 CR12 CR13	DIODE	1N4148	FAIR	4807-02-6666	31

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — PAGE: 10 — REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q15 Q3 Q5	TRANS	2N5485	MOT	4901-05-4850	3
Q12 Q14 Q22 Q25 Q28 Q29 Q31 Q7 Q8	TRANS	2N5771	NSC	4901-05-7710	9
R145	THERMISTER	1K-501-K	MCI	5300-00-0011	1
U9	IC	TL083CN	TI	7000-00-8300	1
U17 U2 U7	IC	TL084CN	TI	7000-00-8400	3
U20	IC	MLM339P	MOT	7000-03-3900	1
U4	IC	NE529	SIG	7000-05-2900	1
U11	IC	CA-3019	FAIR	7000-30-1900	1
U18 U19	IC	CA-3054	RCA	7000-30-5400	2
U15	IC	CA3083	FAIR	7000-30-8300	1
U16 U3	IC	CA-3096AE	RCA	7000-30-9600	2
U1 U10 U12 U8	IC, QUAD SPST CMOS ANALOG SWITCH	D9211CJ	SILX	8000-02-1100	4
U13 U5	IC, QUAD 2-INPUT NAND GATE	74F00	FAIR	8000-74-0002	2
U14	IC, 4-2-3-2 INPUT AND OR-INVERT GATE	74F64	FAIR	8000-74-6402	1
U6	IC, DUAL D-TYPE FLIP-FLOP	74F74	FAIR	8000-74-7402	1

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — PAGE: 12 — REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, FUNCTION GENERATOR
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 271 — DWG NO 1100-00-0920 — REV
	SCALE		CODE IDENT 23338 — SHEET 2 OF 2

BISHOP GRAPH CS/ACCUPRESS REORDER NO A27086

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REV	ECN	BY	DATE	APP
A	#3904	SC	8 883	
—	4154 CLASS III	SC	2-684	
B	ECN 4166	RO	3/84	

MICROPROCESSOR/MEMORY

TEST J8

1 ← E
2 ← ADR15
3
4 ← ADR14
5 ← AS
6 ← ADR13
7
8 ← ADR12
9 ← NMI
10 ← ADR11
11
12 ← ADR10
13
14 ← ADR9
15
16 ← ADR8
17
18 ← AD7
19
20 ← AD6
21
22 ← AD5
23 ← TEST
24 ← AD4
25
26 ← AD3
27 ← +5V
28 ← AD2
29 ← N.C.
30 ← AD1
31 ← N.C.
32 ← AD0
33
34 ← R/W

MICROPROCESSOR

U1A, U1B 1/2 74LS00
U2 I4040
R8 10K SIP
C5 .1/50V
CR3 IN4148
DS1 BEEPER QMB-06
R2 2.49K
Q1 2N3904
C4 .1/50V
C3 27pF
Y1 4MHz
C2 27pF
R1 10K SIP
C1 .001
CR1, CR2 2811(2)
R1 10K SIP
U3 6803
1M (4)
R3, R4, R5, R6
PORT 21, PORT 22, PORT 20, N/C, N/C
PORT 10, PORT 11, PORT 12, PORT 13, PORT 14, PORT 15, PORT 16, PORT 17
P40 ADR8, P41 ADR9, P42 ADR10, P43 ADR11, P44 ADR12, P45 ADR13, P46 ADR14, P47 ADR15
NMI, IRQ
R32 2.2K SIP
R7 2.2K SIP
VSS

ADDRESS LATCH

R8 10K SIP
C6 .1/50V
R7 2.2K SIP
U4 74LS373
P30 AD0, P31 AD1, P32 AD2, P33 AD3, P34 AD4, P35 AD5, P36 AD6, P37 AD7
ADR0, ADR1, ADR2, ADR3, ADR4, ADR5, ADR6, ADR7

GPIB ADDRESS

R1 10K SIP
R8 10K SIP
SW1
GA0, GA1, GA2, GA3, GA4, FPADEN
C7 .1/50V
U5 74LS240
AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7
ETR

DATA LATCH

C47 .1/50V
R32 2.2K SIP
U25 74LS373
AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7
DATA0, DATA1, DATA2, DATA3, DATA4, DATA5, DATA6, DATA7

ROM

U9, U10
ROM1, ROM2
ADR0, ADR1, ADR2, ADR3, ADR4, ADR5, ADR6, ADR7, ADR8, ADR9, ADR10, ADR11, ADR12
C16 .1/50V
C17 .1/50V

RAM

U11, U12 6116L
RAM1, RAM2
R11 2.21K
R12 2.21K
C18 .1/50V
C19 .1/50V
RAM PWR (2A2)

WRITE PULSE

C15 .1/50V
U1D, U1C 1/2 74LS00
R/W, E
WRP

ADDRESS DECODER

R55 10K
R13 2.2K SIP
U13
KYBD, DISP, GPIB, RAM2, ROM2, RAM1, ANALOG
P/N 8600-00-0237

6. PROM'S PROGRAMMED PER MODEL, SEE PARTS LIST.
5. LAST REFERENCE DESIGNATORS USED ARE: R61, C72, CR19, VR4, SW1, U29, Q2, BT1
4. ALL CAPACITORS ARE SHOWN IN MICRO-FARADS.
3. ALL RESISTORS ARE SHOWN IN OHMS.
2. ALL DIODES ARE FD6666.
1. REFERENCE DESIGNATORS SHOWN ARE PARTIAL, PREFIX WITH ASSEMBLY REF DES (A6).

NOTE "UNLESS OTHERWISE SPECIFIED"

GPIB INTERFACE

IEEE-488 INTERFACE

U6 68488
MR, RESET, T/R, CLK, D0, D1, D2, D3, D4, D5, D6, D7, CS, R/W, RS0, RS1, RS2, ASE, IRQ, DMA
C8 .1/50V

ALTERNATE BUS DRIVERS

U7A 75160A
U8A 75161A
C9 .1/50V
C10 .1/50V
C11 .1/50V
C12 .1/50V
R9 100
R10 100
IEEE-488 CONN J2
1 DIO1, 2 DIO2, 3 DIO3, 4 DIO4, 13 DIO5, 14 DIO6, 15 DIO7, 16 DIO8
REN, IFC, DAC, RFD, DAV, EOI, ATN, SRQ
PORT 20

IEE 488 BUS DRIVERS

U7B 3447
U8B 3447
C13 .1/50V
C14 .1/50V
IEEE-488 CONN J2
U6-28, U6-25, U6-16, U6-36, U6-34, U6-30, U6-17, U8A-18, U6-27, U6-23, U6-35, U6-33, U6-31, U6-29, U6-18, U8A-19, U6-26
18,19,20,21,22,23,24

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.CHERMACK	DATE 8-8-83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR RB6		TITLE: SCHEMATIC MICRO PROC/POWER SUPPLY BOARD (A6)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030 ANGLES ± 1		
	DO NOT SCALE DWG		MODEL NO 270 SERIES / DWG NO 0103-00-1094 / REV B
	SCALE		CODE IDENT 23338 / SHEET 1 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3984

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SAMPLE AND HOLD

DAC

-10.24V REF
R17 6.81K
R15 10K
R16 200
+15V
U16B TL082
-10.24 REF ADJ
C22 .1/50V +15V
-10.24V
TP1
ADRØ
U15 DAC 1006
DATAØ
DATA 1
DATA 2
DATA 3
DATA 4
DATA 5
DATA 6
DATA 7
C23 .1/50V +15V
U16A TL082
C24 .1/50V -15V

ANALOG DECODER

+5V
R14 2.2K SIP
ADR 3
ADR 4
ANALOG
U14A 1/2 LS139
ANAØ
ANA1
ANA2
ANA3
C21 .1/50V +5V
U14B 1/2 LS139
ADRØ
ADR 1
ARØ
AR1
AR2
AR3

SAMPLE AND HOLD

C25 .1/50V +15V +5V
1/4 DG211
U17A
C26 .1/50V -15V
C20 .1/50V +5V
R18 301K
R19 301K
C27 22pF
C28 1 mf POLYE
C29 910 pF SM
C30 910 pF SM
U18F LS04
TL082
U19B
C64 .1/50V +15V
C65 .1/50V -15V
U17D
C31 22pF
U18A LS04
R20 301K
R21 301K
C32 .1 POLYE
C33 910 pF SM
C34 910 pF SM
U19A TL082
U17B
C35 22pF
U18C LS04
R22 301K
R23 301K
C36 .1 POLYE
C37 910 pF SM
C38 910 pF SM
U20A TL082
C66 .1/50V +15V
C67 .1/50V -15V
U17C
C39 22pF
U18D LS04
R24 301K
R25 301K
C40 .1 POLYE
C41 910 pF SM
C42 910 pF SM
U20B TL082

BATTERY TEST AND RESET

+5V
C71 .1/50V
R59 499
R57 1M
CR18 2811(2)
C72 .1/50V
R58 1M
CR19
U27B TL082
R61 10K
R60 10K
MR
Q2 2N3904
CR17
CR6
PORT 15
+15V
R29 27.4K
BATV
R26 12.4K
R28 2.37K
U27A TL082
R27 1M
-15V
R30 10K
+5V
R31 3.83K
PORT 14
R56 6.49K
RAM PWR (1A5)

DISPLAY

J7

1	+45V
2	
3	
4	
5	
6	
7	+5V
8	KYBD
9	PORT 21
10	PORT 16
11	DISP
12	
13	AD4
14	AD3
15	AD2
16	AD1
17	ADØ
18	ADR 3
19	ADR 2
20	ADR 1
21	ADRØ
22	
23	DATA 7
24	DATA 6
25	DATA 5
26	DATA 4
27	DATA 3
28	DATA 2
29	DATA 1
30	DATA Ø
31	
32	
33	
34	+15V.

NOTE. UNLESS OTHERWISE SPECIFIED

AUX BUFFERS

+5V
U29 LS244

DATA Ø	B DATA Ø
DATA 1	B DATA 1
DATA 2	B DATA 2
DATA 3	B DATA 3
DATA 4	B DATA 4
DATA 5	B DATA 5
DATA 6	B DATA 6
DATA 7	B DATA 7

U28 LS244

PORT 12	N.C.
N.C.	N.C.
N.C.	N.C.
ADR Ø	B ADRØ
ADR 1	B ADR 1
ADR 2	B ADR 2
N.C.	N.C.

ANALOG REGISTERS

U21 C374

DATA Ø	ANLØ
DATA 1	ANL1
DATA 2	ANL2
DATA 3	ANL3
DATA 4	ANL4
DATA 5	ANL5
DATA 6	ANL6
DATA 7	ANL7

U22 C374

DATA Ø	ANL8
DATA 1	ANL9
DATA 2	ANL10
DATA 3	ANL11
DATA 4	ANL12
DATA 5	ANL13
DATA 6	ANL14
DATA 7	ANL15

U23 C374

DATA Ø	ANL16
DATA 1	ANL17
DATA 2	ANL18
DATA 3	ANL19
DATA 4	ANL20
DATA 5	ANL21
DATA 6	ANL22
DATA 7	ANL23

U24 C374

DATA Ø	ANL24
DATA 1	ANL25
DATA 2	ANL26
DATA 3	ANL27
DATA 4	
DATA 5	
DATA 6	
DATA 7	

C43 C44 C45 C46 .1/50V +5V

ANALOG

J6

SHØ	1
SH1	2
SH2	3
SH3	4
ANLØ	5
ANL1	6
ANL2	7
ANL3	8
ANL4	9
ANL5	10
ANL6	11
ANL7	12
ANL8	13
ANL9	14
ANL10	15
ANL11	16
ANL12	17
ANL13	18
ANL14	19
ANL15	20
ANL16	21
ANL17	22
ANL18	23
ANL19	24
ANL20	25
ANL21	26
ANL22	27
ANL23	28
ANL24	29
ANL25	30
ANL26	31
ANL27	32
PORT 10	33
PORT 11	34

AUX

J4

BDATAØ	1
BDATA 1	2
BDATA 2	3
BDATA 3	4
BDATA 4	5
BDATA 5	6
BDATA 6	7
BDATA 7	8
BADR Ø	9
BADR 1	10
BADR 2	11
ANA 2	12
ANA 3	13
	14
	15
	16
	17
	18
	19
PORT 13	20

REV	ECN	BY	DATE	APP

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN S.CHERMACK DATE 1883
PROJ ENGR K.B.G. 7/14/83
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1° XX ± .030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
SCHEMATIC
MICRO PROC/POWER SUPPLY BOARD (A6)

MODEL NO 270 SERIES
DWG NO 0103-00-1094
REV B
CODE IDENT 23338
SHEET 2 OF 3

7-21

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

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POWER SUPPLY

REV	ECN	BY	DATE	APP

TRANSFORMER J1

45 VAC 1
45 VAC 2
15 VAC 3
15 VAC 4
GND 5
N/C 6 — N/C
N/C 7 — N/C
N/C 8 — N/C
5 VAC 9
5 VAC 10

CR7 3N254
CR13 3N254
CR15 3N254

CR8 IN4002
VR1 LM317
R33 1.8, 1/2W, CARB
R34 3.92K
C70 100/25V
R35 499
CR9
R36 3.92 K
C69 .1/50V
U26A ½ TL082
R37 1.21K
R38 2.74K
R39 500
R40 1.78K
CR10 IN823A
R41 10K
C48 4700/25V
C49 .1/50V
C52 .1/50V
C53 1000/16V

CR11
R42 3.92K
U26B ½ TL082
R46 4.99K
R47 200
R48 10K
C50 4700/25V
C51 .1/50V
C54 .1/50V
C55 1000/16V
VR2 LM337
R43 3.92K
C68 100/25V
R44 499
R45 1.8, 1/2W, CARB
CR12 IN4002(2)

CR14
VR3 LM317
R50 1.1K
R53 1K
R49 3.16 K
C56 6800/16V
C57 .1/50V
C58 .1/50V
C59 1000/16V

+5V TEST JUMPER E2 E1

CR16 IN4002
VR4 LM317
R52 301
R54 49.9K
R51 10K
C60 470/50V
C61 .1/50V
C62 .1/50V
C63 470/50V

+45V J7-1 (2A8)

+15V
+15V
-15V
-15V
+5V
+5V

ANALOG POWER J5
1 +15V
2 +15V
3
4
5
6
7
8
9
10

AUX POWER J3
1 +5V
2
3
4
5
6
7
8
9
10

TP2 TP3 TP4 TP5

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. CHERMACK	DATE 8-83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR R. U.	11/15/83	TITLE: SCHEMATIC MICRO PROC/POWER SUPPLY BOARD (A6)
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG		MODEL NO 270 SERIES / DWG NO 0103-00-1094 / REV B
	SCALE		CODE IDENT 23338 / SHEET 3 OF 3

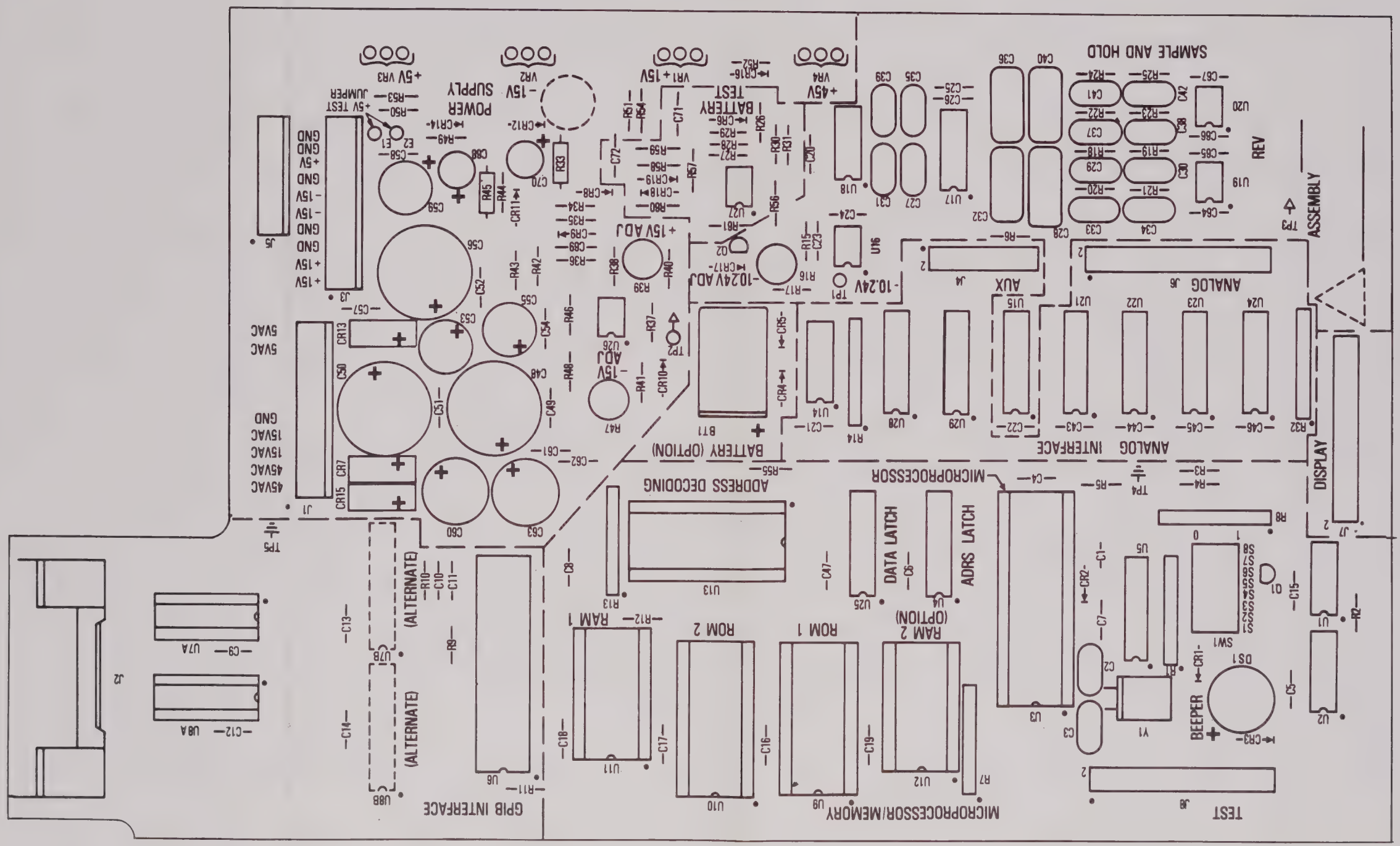
SILHOUETTE GRAPHICS/ACCUPRESS REORDER NO. A-3664

WAVETEK
San Diego - California

TITLE
MICRO PROC/POWER SUPPLY

MODEL NO	ASSY NO	REV
271	1100-00-1094	

CODE IDENT 23338 SHEET 1 OF 1



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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, MICRO-PROC POWER SUPPLY	0101-00-1094	WVTK	0101-00-1094	1
NONE	SCHEMATIC, MICRO-PROC POWER SUPPLY	0103-00-1094	WVTK	0103-00-1094	1
C1	CAP, CER, .001MF, 1KV	DD-102 LONG LEAD	CRL	1500-01-0201	1
C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C4 C43 C44 C45 C46 C47 C49 C5 C51 C52 C54 C57 C58 C6 C61 C62 C64 C65 C66 C67 C69 C7 C71 C72 C8 C9	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	43
C27 C31 C35 C39	CAP, CER, 22PF, 1KV	DD-220	CRL	1500-02-2011	4
C2 C3	CAP, MICA, 27PF, 500V	DM15-270J	ARCO	1500-12-7000	2
C29 C30 C33 C34 C37 C38 C41 C42	CAP, 910PF, 100V, 5%	DM15-911J	ARCO	1500-19-1100	8
C68 C70	CAP, ELECT, 100MF, 25V RADIAL LEAD, SP .20	CRE SERIES 100/25	CAPAR	1500-31-0102	2
C53 C55 C59	CAP, ELECT, 1000MF/16V RADIAL LEAD, SP .20	CRE SERIES 1000/16	CAPAR	1500-31-0211	3
C60 C63	CAP, ELECT, 470MF/50V RADIAL LEAD, SP .30	CRE SERIES 470/50	CAPAR	1500-34-7103	2
C48 C50	CAP, ELECT, 4700MF/25V	CRE SERIES 4700/25	CAPAR	1500-34-7202	2

WAVETEK PARTS LIST | TITLE PCA, MICRO-PROC/ POWER SUPPLY | ASSEMBLY NO. 1100-00-1094 | PAGE: 1 | REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	RADIAL LEAD, SP .50				
C56	CAP, ELECT, 6800MF, 16V RADIAL LEAD, SP .50	CRE SERIES 6800/16	CAPAR	1500-36-8201	1
C32 C36 C40	CAP, MYLAR, .1MF, 100V	225P10491WD3	SPRAG	1500-41-0444	3
C28	CAP, MYLAR, 1MF, 100V	PMT2R1.0K100	ITT	1500-41-0524	1
NONE	MICRO-PROC/GPIB BD	1700-00-1094	WVTK	1700-00-1094	1
J1 J3	CONN HEADER	09-60-1101	MOLEX	2100-02-0088	2
J5	CONNECTOR, HEADER (10 PIN)	1-640456-0	AMP	2100-02-0133	1
J4	CONN, HOUSING, 20 PIN WITH POLARIZING TABS	2100-02-0137	WVTK	2100-02-0137	1
J6 J7	CONN, HOUSING, 34 PIN WITH POLARIZING TABS	2100-02-0138	WVTK	2100-02-0138	2
NONE	SKT, IC, 16PIN	DILB-16P-108	BURND	2100-03-0028	2
NONE	SKT, IC, 24PIN	DILB-24P-108	BURND	2100-03-0029	2
NONE	SKT, IC, 40PIN	DILB-40P-108	BURND	2100-03-0030	1
NONE	SOCKET, 20 PIN	DIBL-20P-108	BURND	2100-03-0051	2
NONE	SKT, IC, 28PIN	DILB-29P-108	BURND	2100-03-0055	3
NONE	SOCKET, 8 PIN	DILB-08P-108	BURND	2100-03-0063	2
NONE	TERM	2000B1	USECO	2100-05-0009	12

WAVETEK PARTS LIST | TITLE PCA, MICRO-PROC/ POWER SUPPLY | ASSEMBLY NO. 1100-00-1094 | PAGE: 2 | REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
TP1 TP2 TP3 TP4 TP5	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	5
J8	HEADER, 34 PIN	929836-01-17	AP	2100-05-0041	1
J2	CONNECTOR, MOD FROM: 2100-02-0126	2100-99-0062	WVTK	2100-99-0062	1
Y1	CRYSTAL, 4MHZ	180-502	WVTK	2300-99-0004	1
NONE	JUMPER	461-2871-01-03-10	CAMB	3000-00-0034	1
E1 E2	PINS, JUMPER	450-3704-01-03	CAMB	3000-00-0035	2
DS1	BEEPER	GMB-06	STMIC	3000-00-0085	1
NONE	BATTERY HOLDER	3000-00-0090	WVTK	3000-00-0090	1
BT1	BATTERY, LITHIUM, 3V	BR-1/2A	PANAS	4000-02-0007	1
R16 R47	POT, TRIM, 200	91AR200	BECK	4600-02-0101	2
R39	POT, TRIM, 500	91AR500	BECK	4600-05-0104	1
R33 R45	RES, C, 1/2W, 5%, 1.8	RC20GF-1R8	STKPL	4700-25-0189	2
R10 R9	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	2
R53	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	1
R15 R30 R41 R48 R51 R55 R60 R61	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	8
R27 R3 R4 R5 R57 R58	RES, MF, 1/8W, 1%, 1M	RN55D-1004F	TRW	4701-03-1004	7

WAVETEK PARTS LIST | TITLE PCA, MICRO-PROC/ POWER SUPPLY | ASSEMBLY NO. 1100-00-1094 | PAGE: 3 | REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R6					
R50	RES, MF, 1/8W, 1%, 1.1K	RN55D-1101F	TRW	4701-03-1101	1
R37	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	1
R26	RES, MF, 1/8W, 1%, 12.4K	RN55D-1242F	TRW	4701-03-1242	1
R40	RES, MF, 1/8W, 1%, 1.78K	RN55D-1781F	TRW	4701-03-1781	1
R11 R12	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	2
R28	RES, MF, 1/8W, 1%, 2.37K	RN55D-2371F	TRW	4701-03-2371	1
R2	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	1
R38	RES, MF, 1/8W, 1%, 2.74K	RN55D-2741F	TRW	4701-03-2741	1
R29	RES, MF, 1/8W, 1%, 27.4K	RN55D-2742F	TRW	4701-03-2742	1
R52	RES, MF, 1/8W, 1%, 301	RN55D-3010F	TRW	4701-03-3010	1
R18 R19 R20 R21 R22 R23 R24 R25	RES, MF, 1/8W, 1%, 301K	RN55D-3013F	TRW	4701-03-3013	8
R49	RES, MF, 1/8W, 1%, 3.16K	RN55D-3161F	TRW	4701-03-3161	1
R31	RES, MF, 1/8W, 1%, 3.83K	RN55D-3831F	TRW	4701-03-3831	1
R34 R36 R42 R43	RES, MF, 1/8W, 1%, 3.92K	RN55D-3921F	TRW	4701-03-3921	4
R35 R44 R59	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	3
R46	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	1

WAVETEK PARTS LIST | TITLE PCA, MICRO-PROC/ POWER SUPPLY | ASSEMBLY NO. 1100-00-1094 | PAGE: 4 | REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R54	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	1
R56	RES, MF, 1/8W, 1%, 6.19K	RN55D-6191F	TRW	4701-03-6191	1
R17	RES, MF, 1/8W, 1%, 6.81K	RN55D-6811F	TRW	4701-03-6811	1
R1 R8	RES MODULE, 10K	4310R-101-103	BOURN	4770-00-0008	2
R13 R14 R32 R7	RES MODULE 2.2K	4310R-101-222	BOURN	4770-00-0011	4
CR10	DIODE, ZENER 6.2V	1N823A	MOT	4801-01-0823	1
CR12 CR14 CR16 CR8	DIODE	1N4002	FAIR	4801-02-0001	4
CR13 CR15 CR7	DIODE	3N254	MOT	4801-02-0254	3
CR4	DIODE	MBR 120	MOT	4806-02-0120	1
CR11 CR17 CR3 CR6 CR9	DIODE	1N4148	FAIR	4807-02-6666	5
CR1 CR18 CR19 CR2 CR5	DIODE	5082-2811	HP	4809-02-2811	5
Q1 Q2	TRANS	2N3904	FAIR	4901-03-9040	2
SW1	SWITCH PC	2400080	EECO	5199-00-0004	1
VR1 VR3 VR4	IC	LM317T	NSC	7000-03-1700	3
VR2	VOLTAGE REGULATOR	LM337T	NAT	7000-03-3700	1
U16 U19 U20 U26 U27	IC, INPUT OP AMP	TL082CP	TI	7000-08-2000	5
U15	IC, DAC	DAC1006LCN	NAT	7000-10-0600	1

WAVETEK PARTS LIST | TITLE PCA, MICRO-PROC/ POWER SUPPLY | ASSEMBLY NO. 1100-00-1094 | PAGE: 5 | REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U17	IC, QUAD SPST CMOS ANALOG SWITCH	DG211CJ	SILX	8000-02-1100	1
U7B U8B	IC	MC3447P3	MOT	8000-34-4700	2
U11 U12	IC	HM6116LP-4	HTACH	8000-61-1600	2
U3	IC	MC6803L	MOT	8000-68-0300	1
U1	IC	74LS00	TI	8000-74-0010	1
U18	IC	74LS04	TI	8000-74-0410	1
U2	IC	14040	RCA	8001-40-4000	1
U6	IC	MC6848BP	MOT	8006-84-8800	1
U14	IC	74LS139	SIG	8007-41-3910	1
U5	IC	74LS240	TI	8007-42-4010	1
U28 U29	IC	74LS244	TI	8007-42-4410	2
U25 U4	IC	74LS373	MOT	8007-43-7310	2
U21 U22 U23 U24	IC	74C374	NAT	8007-43-7430	4

WAVETEK PARTS LIST | TITLE PCA, MICRO-PROC/ POWER SUPPLY | ASSEMBLY NO. 1100-00-1094 | PAGE: 6 | REV B

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, MICRO-PROC/ POWER SUPPLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 271 / DWG NO 1100-00-1094 / REV B
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

BISHOP GRAPHICS INCORPORATED NEURODEX NO. 42/089

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	PROM INSTALLATION DRAWING(MICRO-PROC/P.S.)1100-00-1094	0101-00-1025	WVTK	0101-00-1025	1
A6U13	IC, PROGRAMMED REF: 8008-21-0200	8600-00-0237	WVTK	8600-00-0237	1
A6U9	I.C. PROGRAMMED REF; 8000-27-3200 1007	8600-00-0262	WVTK	8600-00-0262	1
A6U10	I.C. PROGRAMMED REF; 8000-27-6400	8600-00-0263	WVTK	8600-00-0263	1

WAVETEK PARTS LIST	TITLE PROM PACKAGE	ASSEMBLY NO. 1109-00-0020 PAGE: 1	REV A

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PROM PACKAGE
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ·010 ANGLES ·1 XX ·030		
	DO NOT SCALE DWG	MODEL NO 271	DWG NO 1109-00-0020 REV A
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A2708

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REV	ECN	BY	DATE	APP
A	#3904	SC	8-1083	RS
B	ECN 4136	RO	1-84	RO
C	ECN 4167, 4165	RO	3/84	RO
—	ECN 4304	DC	5/21/84	RO

DATA LATCHES

J16-
BDATAØ
BDATA1
BDATA2
BDATA3
BDATA4
BDATA5
BDATA6
BDATA7
BADRØ
BADR1
BADR2
ANA2
ANA3
N.C
N.C.

+5V
R1 2.2K SIP
R2 2.2K SIP
R2 2.2K SIP
BADRØ (2C7, 3C7)
BADR1 (3C7)
BADR2 (2C7)
ANA3 (2C7, 3C7)
U1 74LS138
C71 .1/50V
C1 .1/50V
C2 .1/50V

U2 74C374
U3 74C374
U4 74C374
U5 74C374
U6 74C374

BURST (B2)
BURST (B1,B2)
DELON (2D4)
DELPLS (2D4)
B8
B9
B10
B11
B12
B13
B14
B15
B0
B1
B2
B3
B4
B5
B6
B7
DR7 (2B4)
DR6 (2B7)
DR5 (2B7)
DR4 (2B7)
WR4 (3B7)
WR7 (3A4)
WR6 (3B7)
WR5 (3B7)
WR3 (3C5)
WR2 (3C5)
DR3 (2C5)
DR2 (2C5)
WR1 (3C5,3B4)
DR1 (2C5,3B4)
DR0 (2C4,2B5)
WR0 (3B5,3C4)

(2D7, 3D7)
CR1 IN823A 6.2V

±10 VOLT REFERENCE

+15V
C3 .1/50V
R3 1.21K 1/2 TL082
R4 1K
U7B
+VR 10V
R6 40.2K
R5 63.4K
C4 100pF
R7 100K
C5 100pF
R8 100K
1/2 TL082
U7A
-VR 10V
C6 .1/50V
R9 1K
-15V

BURST CONTROL

J15-
N.C.
N.C.
TRGI
TRGO
PLSI (3D2)
SQS (2D4)

U8C
1/2 74F00
U8D
R84 TRIM
R85 TRIM
C7 .1/50V
C9 .1/50V
C10 .1/50V
C11 .1/50V
C12 .1/50V

U9 74LS161
U10 74LS161
U11 74LS161
U12 74LS161
U13 74LS161
U14 74LS133

BURST (CG)
R10 392
U15A
74F74
U15B
C13 100pF
C14 .1/50V
U8B
1/2 74F00
U8A
BURST (CG)
BURST (CG)

COUNTERS

COUNT COMPLETE LOGIC

TP13 TP14 TP15 TP16

J17-
N.C.
N.C.
+15V
-15V
C15 100/16V
C16 100/16V
C17 100/16V

BURST COUNTER

5. * NOMINAL VALUE CALLED OUT ON PARTS LIST
4. ALL DIODES ARE FD 6666.
3. ALL CAPACITORS ARE IN MICRO FARADS.
2. ALL RESISTORS ARE IN OHMS.
1. REFERENCE DESIGNATORS SHOWN ARE PARTIAL PREFIX WITH ASSEMBLY REF DES (A10)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN CHERMACK
DATE 2-2282
PROJENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA
TITLE
SCHEMATIC, PULSE BOARD (A10)
MODEL NO 271
DWG NO 0103-00-0991
REV C
CODE IDENT 23338
SHEET 1 OF 3

BISHOP GRAPHICS/ACCUPRESS RECORDER NO A-3884

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REV	ECN	BY	DATE	APP

DELAY DAC

(1D3) BDATA 7, BDATA 6, BDATA 5, BDATA 4, BDATA 3, BDATA 2, BDATA 1, BDATA 0

+VR 10V, C42 .1/50V, U16 DAC 1006, 1/4 TL084 U17A, C18 .1/50V, C19 .1/50V, -15V, +15V

EADR0 (1D7), BADR2 (1D7), AMA3 (1D7)

TP1

DELAY RANGE CALIBRATION

C68 .1/50V +15V, C66 .1/50V, C67 .1/50V, DG211 U18, DG211 U19

DRØ (1C3), 9.99µs ADJ., R14 100K, U18A DG211

9.99ms ADJ., R15 100K, U18D DG211, DR1 (1C3)

R16 10M, U19D DG211, DR2 (1C3)

R17 750K, U19A DG211, DR3 (1C3)

R12 249K, R13 10K +VR, 139ns ADJ.

R18 301K, 1/4 TL084 U17D, R19 499K, R20 3.01K

R21 100K 1ms ADJ. +VR -VR, DRØ (1C3)

TP2

COMPARATOR LOGIC

DELPLS (1C6), DELON (1C6), SQS (1B7)

R22 2.49K, R23 619, C20 .1/50V, R24 100

U20D DG211, R25 15K, R26 750, C22 .1/50V

C21 10pF, R27 100, NE521 U21A, NE521 U21B

CR2 IN4740A 10V, C23 .1/50V, -15V

TP3

74LF74 U22A, 74LF74 U22B

DOUBLE PULSE LOGIC

C25 .1/50V, C26 10pF, R29 1K, U23A 74F00, U23D 74F00, R30 750

DELTOWID (3D3)

R28 750

DELAY ONE SHOT

DG211 U20

RAMP ENABLE

FAST RESET

RAMP HOLD

CR6 IN823A 6.2V

TP6

TP5

3 DECADE CURRENT SOURCE

C27 .1/50V, R33 249K, R34 249K, R35 2.37K

DG211 U20C, DG211 U20B, DG211 U20A

DR4 (1C4), DR5 (1C4), DR6 (1C4)

TP4

R31 10K, C29 220pF, U24A, Q1 J177

R32 20K, ½ TL082, Q2 2N5462, C28 .1/50V

RAMP RESET

CR3 FD777, C30 10pF, C31 3.5-13pF, CR4 FD777, 1.04µs ADJ., CR5, R84 10

CR7 FD777, CR8, CR9

Q3 2N5484, C32 22pF

R36 4.99K, R37 3.01K, R38 1K, CR10, CR11, R39 4.99K

C69 .1/50V, C33 .1/50V

RANGE CAPACITORS

C34 68 pF S.M.

C35 .01 100V MYLAR, C36 1 100V MYLAR, K1, K2

DRI (1C3), R40 3.01K, Q4, Q5 2N3906 (2)

DR7 (1C4), R41 3.01K, K1, K2, C70 .1/50V

FET BUFFER

C37 .1/50V +15V, U24B ½ TL082, C38 .1/50V -15V

C39 1/50V, Q6 2N5485, C40 .1/50V, R44 100, R47 10, Q8 2N3563, C70 .1/50V

R42 4.64K, Q7 2N3904, R43 7.5K

R45 10K, R46 3.01K, R48 4.99K, C41 .1/50V -15V

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 2-24-88	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC, PULSE BOARD (A10)
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	SCALE	MODEL NO 271 · DWG NO 0103-00-0991 · REV C
			CODE IDENT 23338 · SHEET 2 OF 3

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REV	ECN	BY	DATE	APP

WIDTH DAC

(1D3) BDATA 7 BDATA 6 BDATA 5 BDATA 4 BDATA 3 BDATA 2 BDATA 1 BDATA 0

U25 DAC 1006

+VR 10V

BADR0 (1D7) BADR1 (1D7) ANA3 (1D7)

+15V

C64 .1/50V

1/4 TL084 U17B

TP7

WIDTH RANGE CALIBRATION

R49 249K

WR0 (1C3) 9.99µs ADJ. R51 100K U18B DG211

9.99ms ADJ. R52 100K U18C DG211

WR1 (1C3)

+VR R53 10M U19B DG211

99.9ns ADJ. R50 10K

WR2 (1C3)

R54 750K U19C DG211

WR3 (1C3)

R55 501K

1/4 TL084 U17C

R56 499K

R57 3.01K

TP8

+VR R58 100K 1ms ADJ. -VR

WR0 (1C3)

DELTOWID (2C1)

R59 2.49K R60 619 C43 .1/50V

R61 100

C44 10pF R64 100

+5V NE521 U27A 3,7,10

+15V U26D DG211

R62 15K R63 * C45 .1/50V

+5V NE521 U27B

CR12 1N4740A 10V C46 .1/50V -15V

C47 .1/50V

+5V U28 A 74F74

74F74 U28 B

R65 750

TP9

PLSI(1B7)

WIDTH ONE SHOT

+15V U26 -15V +5V

+15V C48 1/50V

R68 249K R69 249K R70 2.37K

DG211 U26C DG211 U26A DG211 U26B

WR4 (1C4) WR5 (1C4) WR6 (1C4)

TP10

R66 10K R67 20K

C50 220pF

U29B ½ TL082 Q9 J177

Q10 2N5462

C49 .1/50V

CR13 FD777

C51 5pF C52 3.5-43pF

CR14 FD777 1µs ADJ. CR15 R85 10

R71 4.99K

CR17 FD777 CR18 CR19

R72 3.01K

Q11 2N5484

C53 22pF

R73 1K

CR20 CR21

R74 4.99K

C54 .1/50V

-15V

C55 68 pF S.M.

C56 .01/100V MYLAR K3

C57 1/100V MYLAR K4

TP11

C58 .1/50V +15V

U29A ½ TL082

-15V C59 .1/50V

WR1 (1C3) R75 3.01K

WR7 (1C4) R76 3.01K

Q12 Q13 2N3906 (2)

C65 .1/50V

K3 K4

+5V

R77 4.64K R78 7.5K

Q14 2N5485

C60 1/50V C61 .1/50V R79 100

Q15 2N3904

R80 10K R81 3.01K

C62 .1/50V

C63 .1/50V R82 10 Q16 2N3563

R83 4.99K

+15V CR16 1N823A 6.2V

TP12

3 DECADE CURRENT SOURCE

RAMP RESET

RANGE CAPACITORS

FET BUFFER

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 2-24-82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC, PULSE BOARD (A10)
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG		MODEL NO 271 / DWG NO 0103-00-0991 / REV C
	SCALE		CODE IDENT 23338 / SHEET 3 OF 3

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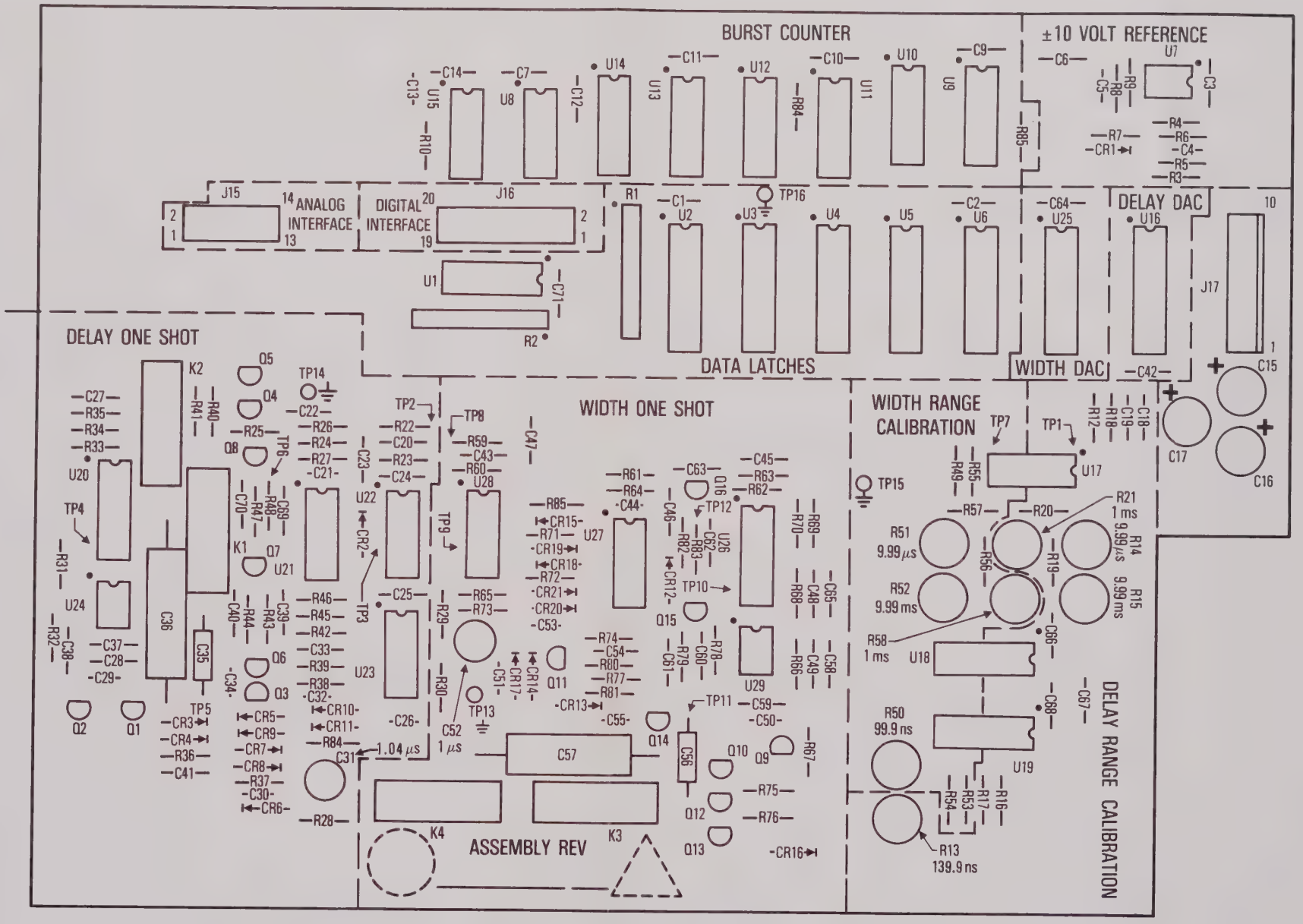

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PULSE BOARD ASSEMBLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES 1 XX .030		
	DO NOT SCALE DWG		MODEL NO 271 · DWG NO 1100-00-0991 · REV
	SCALE		CODE IDENT 23338 · SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, PULSE BD	0101-00-0991	WVTK	0101-00-0991	1
NONE	SCHEMATIC, PULSE BD	0103-00-0991	WVTK	0103-00-0991	1
NONE	ASSY, AUX BOARD SHIELD	270-1020	WVTK	1206-00-1020	1
C51	CAP, CER, 5PF, 1KV	DD-050 LONG LEAD	CRL	1500-00-5001	1
C30	CAP, CER, 10PF, 1KV	DD-100LL	CRL	1500-01-0001	1
C21 C26 C44	CAP, CER, 10PF, 1KV	DD-100	CRL	1500-01-0011	3
C13 C4 C5	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	3
C1 C10 C11 C12 C14 C18 C19 C2 C20 C22 C23 C24 C25 C27 C28 C3 C33 C37 C38 C39 C40 C41 C42 C43 C45 C46 C47 C48 C49 C54 C58 C59 C6 C60 C61 C62 C63 C64 C65 C66 C67 C68 C69 C7 C70 C71 C9	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNO	1500-01-0405	47
C32 C53	CAP, CER, 22PF, 1KV	DD-220	CRL	1500-02-2011	2
C29 C50	CAP, CER, 220PF, 1KV	DD-221	CRL	1500-02-2111	2
C34T C55T	CAP, MICA, 68PF, 500V	DM15-680J	ARCO	1500-16-8000	2
C15 C16 C17	CAP, ELECT, 100MF, 25V RADIAL LEAD, SP .20	CRE SERIES 100/25	CAPAR	1500-31-0102	3

WAVETEK PARTS LIST | TITLE PCA, PULSE BOARD | ASSEMBLY NO. 1100-00-0991 PAGE: 1 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R7 R8	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	2
R47 R82 R84 R85	RES, MF, 1/8W, 1%, 10	RN55D-10R0F	TRW	4701-03-1009	4
R3	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	1
R25 R62	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	2
R32 R67	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	2
R35 R70	RES, MF, 1/8W, 1%, 2.37K	RN55D-2371F	TRW	4701-03-2371	2
R22 R59	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	2
R34 R69	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	2
R12 R33 R49 R68	RES, MF, 1/8W, 249K	RN55D-2493F	TRW	4701-03-2493	4
R20 R37 R40 R41 R46 R57 R72 R75 R76 R81	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	10
R18 R55	RES, MF, 1/8W, 1%, 301K	RN55D-3013F	TRW	4701-03-3013	2
R10	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	1
R6	RES, MF, 1/8W, 1%, 40.2K	RN55D-4022F	TRW	4701-03-4022	1
R42 R77	RES, MF, 1/8W, 1%, 4.64K	RN55D-4641F	TRW	4701-03-4641	2
R36 R39 R48 R71 R74 R83	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	6
R19 R56	RES, MF, 1/8W, 1%, 499K	RN55D-4993F	TRW	4701-03-4993	2

WAVETEK PARTS LIST | TITLE PCA, PULSE BOARD | ASSEMBLY NO. 1100-00-0991 PAGE: 3 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q14 Q6	TRANS	2N5485	MOT	4901-05-4850	2
Q1 Q9	TRANS	J177	SILX	4902-00-1770	2
W15	RIBBON CABLE (3 INCH)	6002-00-0018	WVTK	6002-00-0018	1
W13	RIBBON CABLE (7 INCH)	6002-00-0019	WVTK	6002-00-0019	1
U17	IC	TL084CN	TI	7000-00-8400	1
U21 U27	IC, DUAL DIFFERENTIAL COMPARATOR/SENSE AMP	NE521	SIG	7000-05-2100	2
U24 U29 U7	IC, INPUT OP AMP	TL082CP	TI	7000-08-2000	3
U16 U25	IC, DAC	DAC1006LCN	NAT	7000-10-0600	2
U18 U19 U20 U26	IC, QUAD SPST CMOS ANALOG SWITCH	D0211CJ	SILX	8000-02-1100	4
U23 U8	IC, QUAD 2-INPUT NAND GATE	74F00	FAIR	8000-74-0002	2
U15 U22 U28	IC, DUAL D-TYPE FLIP-FLOP	74F74	FAIR	8000-74-7402	3
U14	IC, 13-INPUT POSITIVE NAND GATE	74S133	TI	8007-41-3301	1
U1	IC	74LS138	TI	8007-41-3810	1
U10 U11 U12 U13 U9	IC	74LS161	SIG	8007-41-6110	5

WAVETEK PARTS LIST | TITLE PCA, PULSE BOARD | ASSEMBLY NO. 1100-00-0991 PAGE: 5 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C35 C56	CAP, POLYC, .01MF, 100V	PA2B103F	ELCUB	1300-41-0304	2
C36 C57	CAP, POLYC, 1MF, 100V	210-81C-105F	IMB	1300-41-0504	2
C31 C52	VARI, 3.5-13PF, 250V	7S-TRIKO-02 3.5/13PF	TRIKO	1300-51-3000	2
NONE	PULSE BOARD	1700-00-0991	WVTK	1700-00-0991	1
J17	CONNECTOR, HEADER (10 PIN)	1-640456-0	AMP	2100-02-0133	1
J15	CONN, HOUSING, 14 PIN WITH POLARIZING TABS	2100-02-0136	WVTK	2100-02-0136	1
J16	CONN, HOUSING, 20 PIN WITH POLARIZING TABS	2100-02-0137	WVTK	2100-02-0137	1
TP13 TP14 TP15 TP16	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	4
NONE	CABLE CLAMP	832	SMITH	2800-00-0009	1
K1 K2 K3 K4	RELAY, REED, FORM-A	RA3019-1051	ETROL	4500-00-0007	4
R13 R50	POT, TRIM, 10K	91AR10K	BECK	4600-01-0315	2
R14 R15 R21 R51 R52 R58	POT, TRIM, 100K	91AR100K	BECK	4600-01-0402	6
R24 R27 R44 R61 R64 R79	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	6
R29 R38 R4 R73 R9	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	5
R31 R45 R66 R80	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	4

WAVETEK PARTS LIST | TITLE PCA, PULSE BOARD | ASSEMBLY NO. 1100-00-0991 PAGE: 2 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R23 R60 R63	RES, MF, 1/8W, 1%, 619	RN55D-6190F	TRW	4701-03-6190	3
R5	RES, MF, 1/8W, 1%, 63.4K	RN55D-6342F	TRW	4701-03-6342	1
R26 R28 R30 R65	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	4
R43 R78	RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	2
R17 R54	RES, MF, 1/4W, 1%, 750K	RN60D-7503F	TRW	4701-13-7503	2
R1 R2	RES MODULE 2.2K	4310R-101-222	BOURN	4770-00-0011	2
R16 R53	RES, MF, 1/4W, 1%, 10M	CC1005F	AB	4799-00-0056	2
CR1 CR16 CR6	DIODE, ZENER 6.2V	1N823A	MOT	4801-01-0823	3
CR12 CR2	DIODE	1N4740A	MOT	4801-01-4740	2
CR13 CR14 CR17 CR3 CR4 CR7	DIODE	FD777	FAIR	4807-02-0777	6
CR10 CR11 CR15 CR18 CR19 CR20 CR21 CR5 CR8 CR9	DIODE	1N4148	FAIR	4807-02-6666	10
Q16 Q8	TRANS	2N3563	FAIR	4901-03-5630	2
Q15 Q7	TRANS	2N3904	FAIR	4901-03-9040	2
Q12 Q13 Q4 Q5	TRANS	2N3906	FAIR	4901-03-9060	4
Q10 Q2	TRANS	2N5462	MOT	4901-05-4620	2
Q11 Q3	TRANS	2N5484	MOT	4901-05-4840	2

WAVETEK PARTS LIST | TITLE PCA, PULSE BOARD | ASSEMBLY NO. 1100-00-0991 PAGE: 4 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U2 U3 U4 U5 U6	IC	74C374	NAT	8007-43-7430	5

WAVETEK PARTS LIST | TITLE PCA, PULSE BOARD | ASSEMBLY NO. 1100-00-0991 PAGE: 6 | REV D

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, PULSE BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES :1 XX .030		
	DO NOT SCALE DWG		MODEL NO 271 / DWG NO 1100-00-0991 / REV D
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

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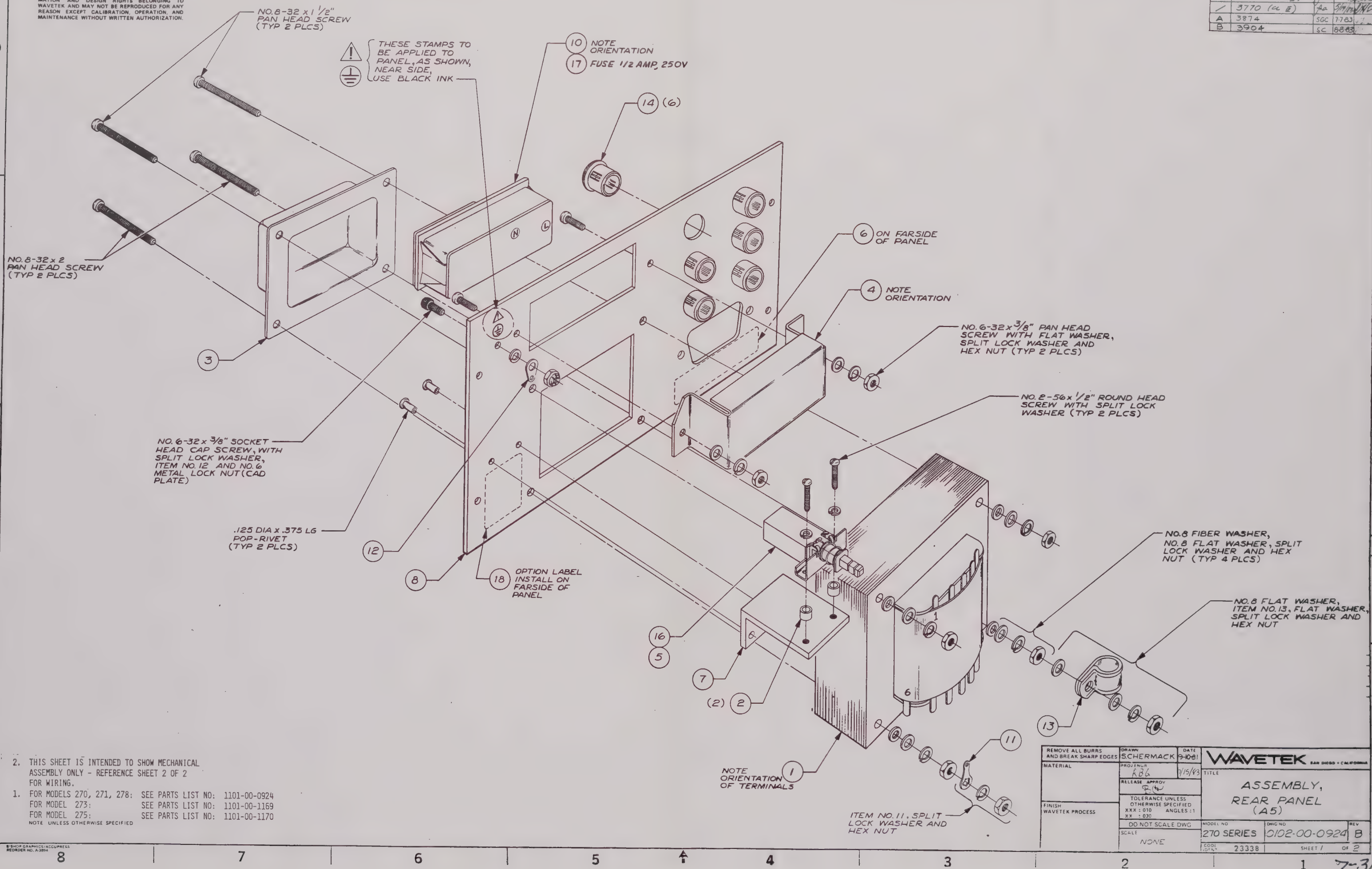
REV	ECN	BY	DATE	APP
/	3756 (cc II)	fha	5/11/82	
/	3770 (cc E)	fha	5/19/82	
A	3874	SGC	7-7-83	
B	3904	SC	8-8-83	


NO.8-32 x 1 1/2" PAN HEAD SCREW (TYP 2 PLCS)
THESE STAMPS TO BE APPLIED TO PANEL, AS SHOWN, NEAR SIDE, USE BLACK INK
10 NOTE ORIENTATION
17 FUSE 1/2 AMP, 250V
14 (6)
NO.8-32 x 2 PAN HEAD SCREW (TYP 2 PLCS)
6 ON FARSIDE OF PANEL
4 NOTE ORIENTATION
NO.6-32 x 3/8" PAN HEAD SCREW WITH FLAT WASHER, SPLIT LOCK WASHER AND HEX NUT (TYP 2 PLCS)
NO.2-56 x 1/2" ROUND HEAD SCREW WITH SPLIT LOCK WASHER (TYP 2 PLCS)
3
NO.6-32 x 3/8" SOCKET HEAD CAP SCREW, WITH SPLIT LOCK WASHER, ITEM NO.12 AND NO.6 METAL LOCK NUT (CAD PLATE)
.125 DIA x .375 LG POP-RIVET (TYP 2 PLCS)
12
8
18 OPTION LABEL INSTALL ON FARSIDE OF PANEL
NO.8 FIBER WASHER, NO.8 FLAT WASHER, SPLIT LOCK WASHER AND HEX NUT (TYP 4 PLCS)
NO.8 FLAT WASHER, ITEM NO.13, FLAT WASHER, SPLIT LOCK WASHER AND HEX NUT
16
5
7
(2) 2
13
11
1
NOTE ORIENTATION OF TERMINALS
ITEM NO.11, SPLIT LOCK WASHER AND HEX NUT

2. THIS SHEET IS INTENDED TO SHOW MECHANICAL ASSEMBLY ONLY - REFERENCE SHEET 2 OF 2 FOR WIRING.
1. FOR MODELS 270, 271, 278: SEE PARTS LIST NO: 1101-00-0924
   FOR MODEL 273: SEE PARTS LIST NO: 1101-00-1169
   FOR MODEL 275: SEE PARTS LIST NO: 1101-00-1170
   NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.CHERMACK	DATE 9-10-81	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR RBG	7/15/93	TITLE ASSEMBLY, REAR PANEL (A5)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 270 SERIES / DWG NO 0102-00-0924 / REV B
	SCALE NONE		CODE IDENT NO 23338 / SHEET 1 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

7-31

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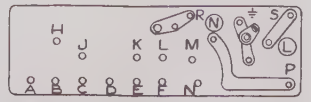
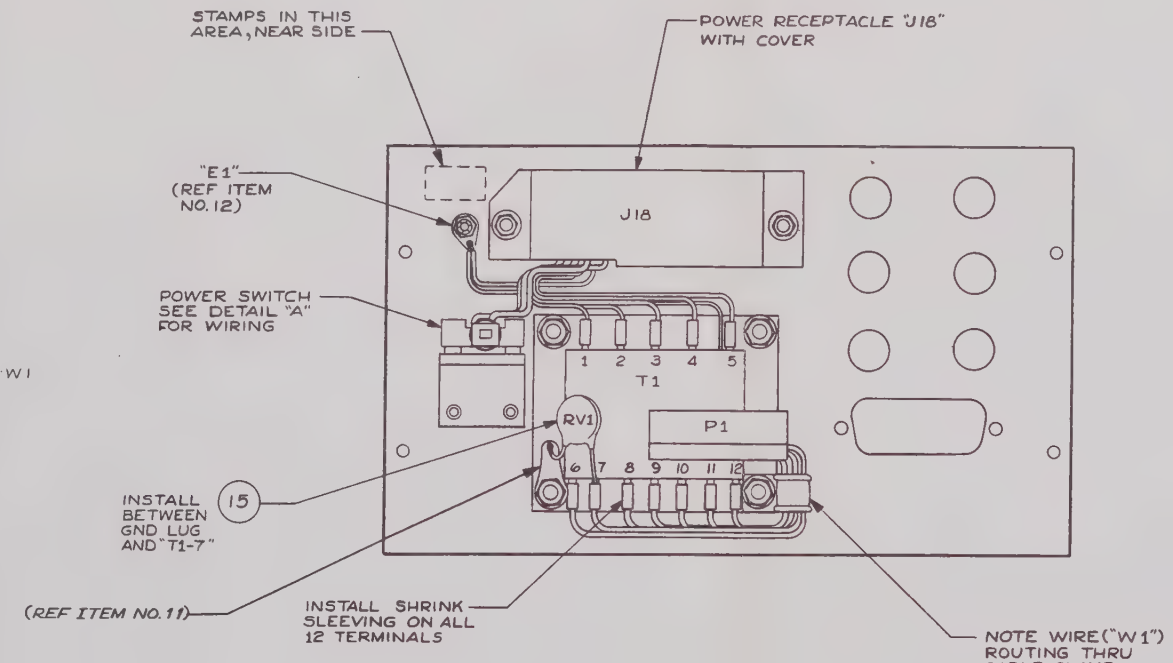
REV	ECN	BY	DATE	APP

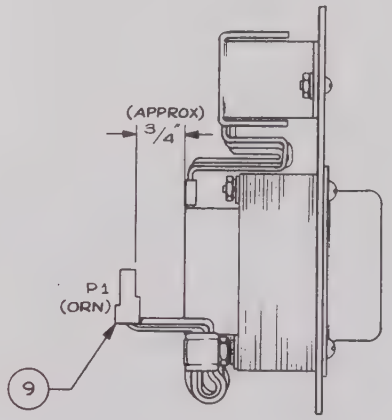


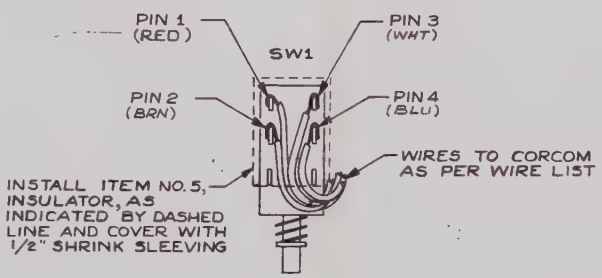
POWER RECEPTACLE PIN MARKING

WIRE LIST

AWG	COLOR	LENGTH	DESTINATION FROM	DESTINATION TO	
18	BLU	4	P1-1	T1-11	W1
18	BLU	4	P1-2	T1-12	
18	GRN	5 1/2	P1-3	T1-6	
18	GRN	5 1/4	P1-4	T1-8	
18	WHT	5 1/2	P1-5	T1-7	
			P1-6		
			P1-7		
			P1-8		
18	RED	5 1/2	P1-9	T1-9	
18	RED	5 1/4	P1-10	T1-10	
22	BLK		J18-C	T1-1	
22	ORN		J18-A	T1-2	
22	WHT/BLK		J18-E	T1-3	
22	GRY		J18-D	T1-4	
22	WHT/GRY		J18-F	T1-5	
22	GRN/YEL		A5-E1	T1(SHIELD)	
22	BUS		J18-B	J18-H	
22	BRN		J18-R	SW1-2	
22	RED		J18-S	SW1-1	
22	BLU		J18-L	SW1-4	
22	WHT		J18-P	SW1-3	
22	GRN/YEL		J18-⏚	A5-E1	

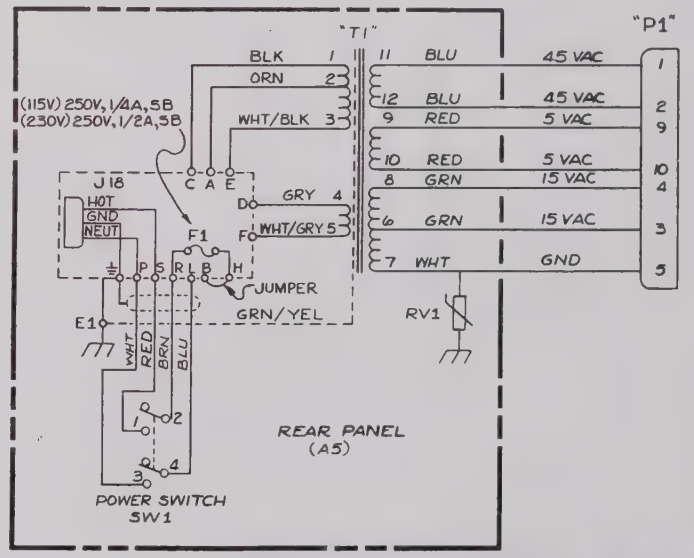

STAMPS IN THIS AREA, NEAR SIDE
POWER RECEPTACLE "J18" WITH COVER
"E1" (REF ITEM NO. 12)
J18
POWER SWITCH SEE DETAIL "A" FOR WIRING
1 2 3 4 5
T1
RV1
P1
6 7 8 9 10 11 12
INSTALL BETWEEN GND LUG AND "T1-7"
15
(REF ITEM NO. 11)
INSTALL SHRINK SLEEVING ON ALL 12 TERMINALS
NOTE WIRE("W1") ROUTING THRU CABLE CLAMP




PIN 1 (RED)
PIN 2 (BRN)
SW1
PIN 3 (WHT)
PIN 4 (BLU)
WIRES TO CORCOM AS PER WIRE LIST
INSTALL ITEM NO. 5, INSULATOR, AS INDICATED BY DASHED LINE AND COVER WITH 1/2" SHRINK SLEEVING

DETAIL "A"

POWER SWITCH WIRING AND INSULATOR ASSY



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 11-5-81	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR RBG	7/15/83	TITLE: ASSEMBLY, REAR PANEL - (A5)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX: 010 ANGLES: 1° XX: 030		
	DO NOT SCALE DWG		MODEL NO 270 SERIES / DWG NO 0102-00-0924 / REV B
	SCALE		CODE IDENT 23338 / SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3804

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, REAR PANEL	0102-00-0924	WVTK	0102-00-0924	1
1	TRANSFORMER	270-0049	WVTK	1204-00-0049	1
2	SPACER	8480	WVTK	1400-00-0653	2
3	END BELL	157-300-EB	WVTK	1400-00-3224	1
4	SHIELD, PWR	1400-00-6210	WVTK	1400-00-6210	1
5	INSULATOR, PWR SWITCH REF: 1600-99-0001	1400-00-8370	WVTK	1400-00-8370	1
6	I.D. LABEL	1400-00-9090	WVTK	1400-00-9090	1
7	BRACKET, SWITCH MNTG	1400-01-3263	WVTK	1400-01-3263	1
8	REAR PANEL FROM: 1400-01-3882	1400-01-3880	WVTK	1400-01-3880	1
18	LABEL, OPTION	1400-01-4960	WVTK	1400-01-4960	1
9	CONNECTOR, HOUSING 18 AWG	1-640431-0	AMP	2100-02-0115	1
10	RECEPTACLE	6VJ1	CORCM	2100-03-0026	1
11	TERM, LOCK LUG	1414-8	SMITH	2100-04-0010	1
12	SOLDER LUG	11A144	ZIER	2100-04-0025	1
17	FUSE, 1/2A, 250V	313.500	LITFU	2400-03-0010	1
13	CLAMP, CABLE	833	SMITH	2800-00-0022	1

WAVETEK PARTS LIST	TITLE ASSY, REAR PANEL	ASSEMBLY NO. 1101-00-0924 PAGE: 1	REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
14	PLUG BUTTON	2643/DP-500 BLACK	HEYCO	2800-35-0003	6
15	VARISTOR	V56ZA8	GE	4799-00-0048	1
16	SWITCH ASSY PB	5103-00-0020	WVTK	5102-00-0005	1

WAVETEK PARTS LIST	TITLE ASSY, REAR PANEL	ASSEMBLY NO. 1101-00-0924 PAGE: 2	REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST ASSY, REAR PANEL
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 271 / DWG NO 1101-00-0924 / REV
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27086

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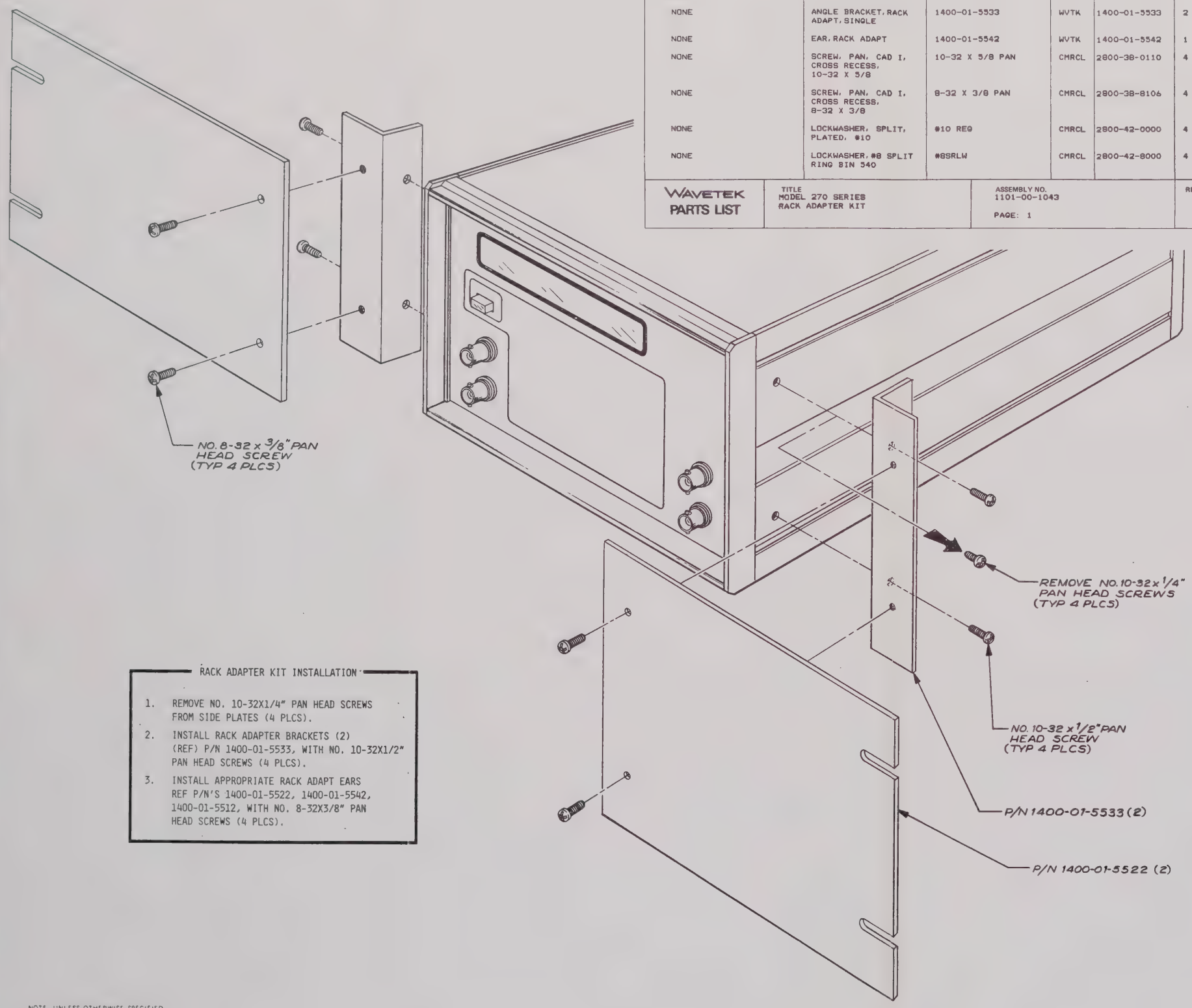
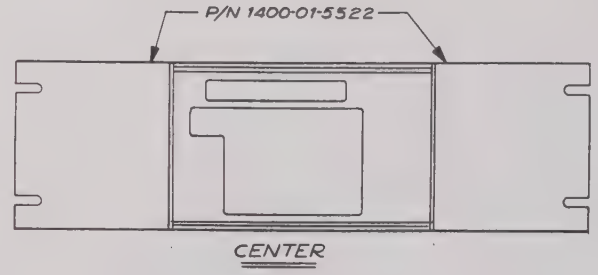
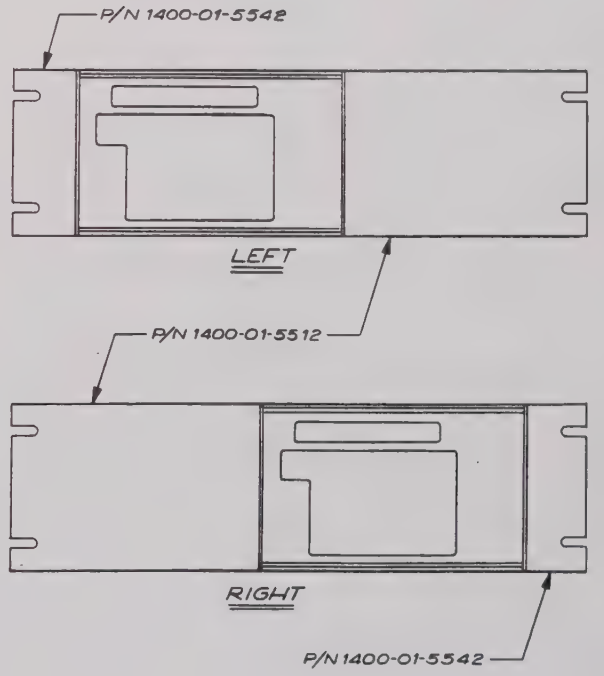
REV	ECN	BY	DATE	APP
A	# 3332	SC	9/1482	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, RACK ADAPTER KIT, SINGLE	0102-00-1043	WVTK	0102-00-1043	1
NONE	EAR, RACK ADAPT	1400-01-5512	WVTK	1400-01-5512	1
NONE	EAR, RACK ADAPT	1400-01-5522	WVTK	1400-01-5522	2
NONE	ANGLE BRACKET, RACK ADAPT, SINGLE	1400-01-5533	WVTK	1400-01-5533	2
NONE	EAR, RACK ADAPT	1400-01-5542	WVTK	1400-01-5542	1
NONE	SCREW, PAN, CAD I, CROSS RECESS, 10-32 X 5/8	10-32 X 5/8 PAN	CMRCL	2800-38-0110	4
NONE	SCREW, PAN, CAD I, CROSS RECESS, 8-32 X 3/8	8-32 X 3/8 PAN	CMRCL	2800-38-8106	4
NONE	LOCKWASHER, SPLIT, PLATED, #10	#10 REQ	CMRCL	2800-42-0000	4
NONE	LOCKWASHER, #8 SPLIT RING BIN 540	#8SRLW	CMRCL	2800-42-8000	4

WAVETEK PARTS LIST | TITLE: MODEL 270 SERIES RACK ADAPTER KIT | ASSEMBLY NO. 1101-00-1043 PAGE: 1 | REV A


NO. 8-32 x 3/8" PAN HEAD SCREW (TYP 4 PLCS)
REMOVE NO. 10-32 x 1/4" PAN HEAD SCREWS (TYP 4 PLCS)
NO. 10-32 x 1/2" PAN HEAD SCREW (TYP 4 PLCS)
P/N 1400-01-5533 (2)
P/N 1400-01-5522 (2)





RACK ADAPTER KIT INSTALLATION

1. REMOVE NO. 10-32X1/4" PAN HEAD SCREWS FROM SIDE PLATES (4 PLCS).
2. INSTALL RACK ADAPTER BRACKETS (2) (REF) P/N 1400-01-5533, WITH NO. 10-32X1/2" PAN HEAD SCREWS (4 PLCS).
3. INSTALL APPROPRIATE RACK ADAPT EARS REF P/N'S 1400-01-5522, 1400-01-5542, 1400-01-5512, WITH NO. 8-32X3/8" PAN HEAD SCREWS (4 PLCS).

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 9-1982	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RBG	7/15/82	TITLE: ASSEMBLY, RACK ADAPTER KIT
	RELEASE APPROV BM		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 XX : 030 ANGLES : 1		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO 0102-00-1043 REV A
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS ACCUPRESS REORDER NO. A 3894

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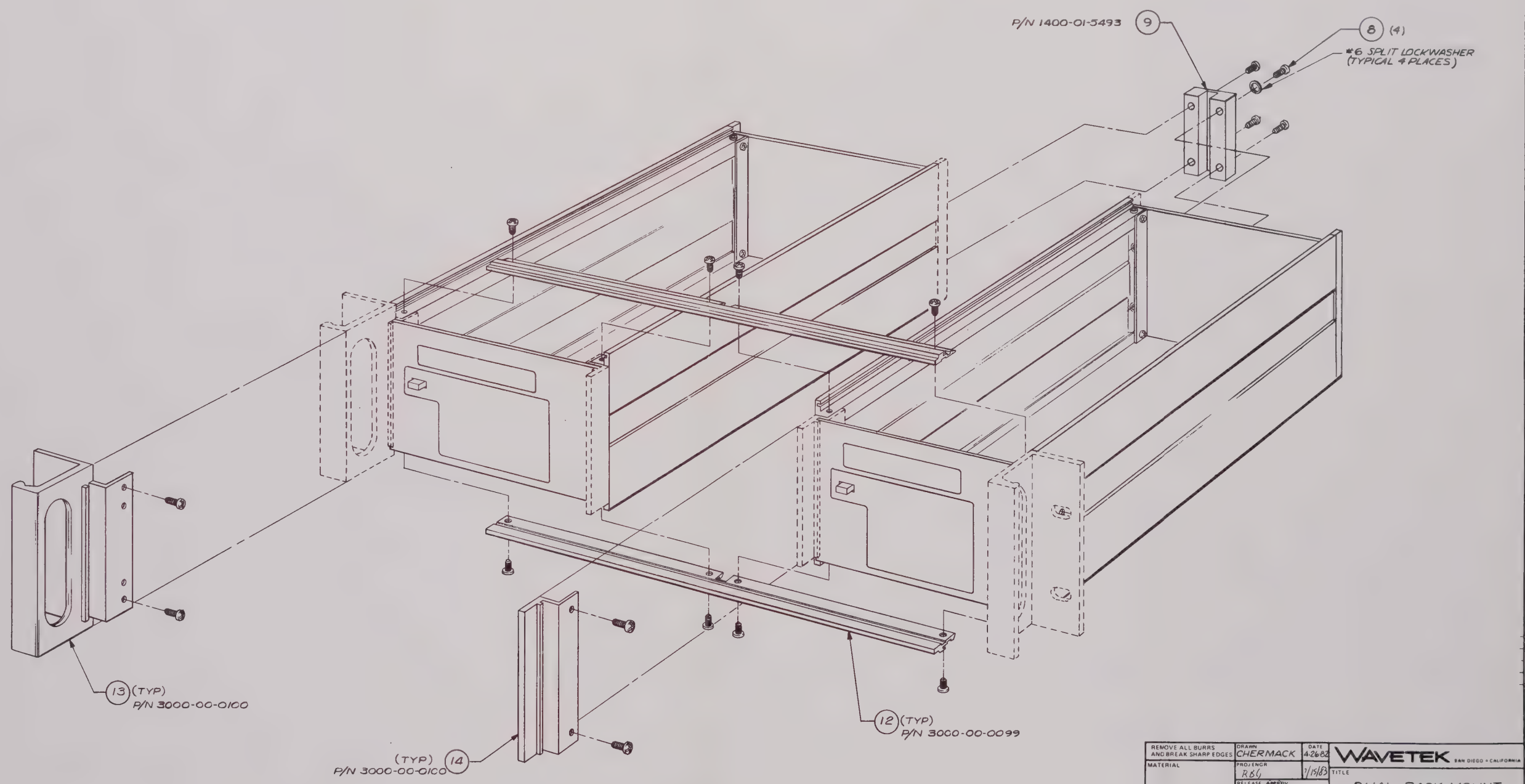
REV	ECN	BY	DATE	APP
A	ECN 4090	RO	3/84	



VIEW "A"

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 4-26-82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR RBG	7/15/83	TITLE: DUAL RACK MOUNT, 270 SERIES
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 270 SERIES; DWG NO 0102-00-1041; REV A
	SCALE NONE		CODE IDENT 23338; SHEET 1 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

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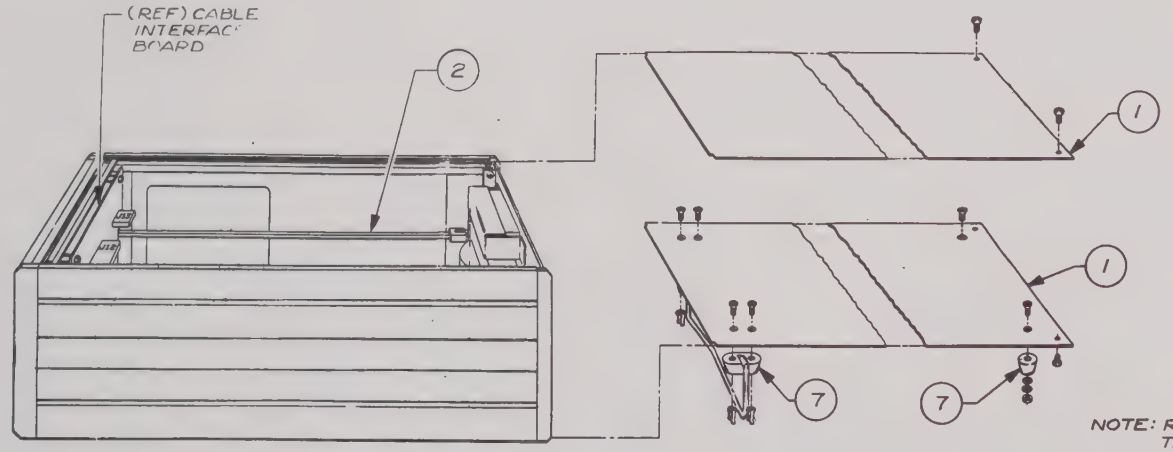
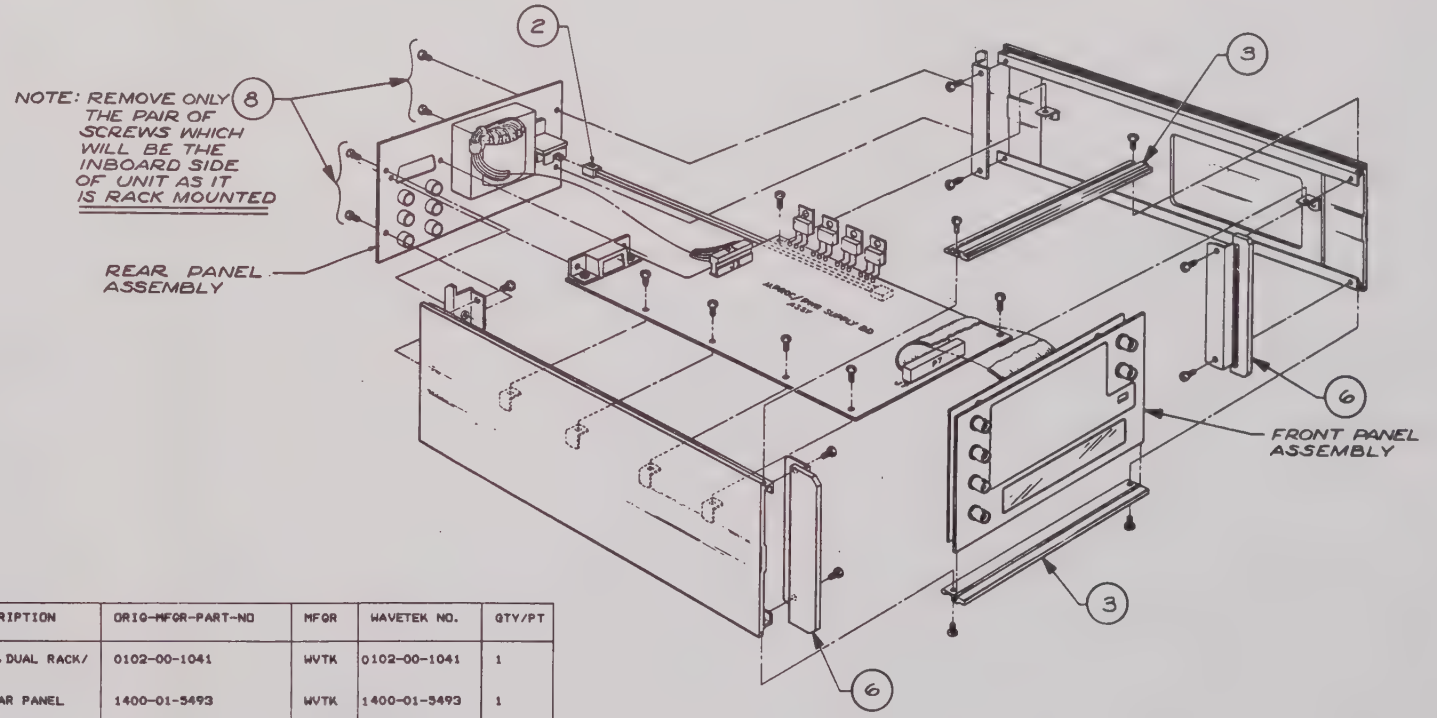
REV	ECN	BY	DATE	APP



VIEW "B"



VIEW "C"

VIEW "C" IS SHOWN WITH UNIT UPSIDE DOWN.

SEQUENCE OF CHANGES FOR DUAL RACK-MOUNTING (USE ORIGINAL SCREWS EXCEPT ITEM 9.)

1. REMOVE TOP AND BOTTOM COVERS (REF ITEMS #1)
2. REMOVE POWER ROD ASSEMBLY (REF ITEM #2) THRU FRONT PANEL ASSEMBLY.
3. REMOVE BOTH TOP AND BOTTOM FRONT HORIZONTAL TRIM PIECES (REF ITEMS #3) TO BE REPLACED BY NEW TRIM (REF ITEMS #12).
4. DISCONNECT PLUGS, "P12" (AND "P13" IF APPLICABLE) FROM CABLE INTERFACE BD., ALSO DISCONNECT "P7" FROM MICROPROC/POWER SUPPLY BOARD.
5. REMOVE FRONT PANEL ASSEMBLY.
6. REMOVE FRONT VERTICAL TRIM PIECES (REF ITEMS #6) AND REPLACE WITH APPROPRIATE REPLACEMENTS (REF ITEM #'S 13 AND 14).
7. REMOVE FEET AND BAIL ASSEMBLY (REF ITEMS #7) FROM BOTTOM COVER, AND REASSEMBLE BY REVERSING STEPS 1 THROUGH 6.
8. REMOVE APPROPRIATE (INBOARD ONLY) REAR PANEL MOUNTING SCREWS (REF ITEMS #8).
9. INSTALL NEW VERTICAL BRACKET (REF ITEM #9) TO REAR PANELS OF UNITS ON INBOARD MOUNTING HOLES. USING SUPPLIED 6-32 x 3/4 SCREWS AND #6 LOCKWASHER.

VIEWS ARE SHOWN TO ILLUSTRATE MECHANICAL BUILD UP OF UNIT PERTAINING TO ITEMS WHICH MUST BE REMOVED AND REPLACED BY NEW ITEMS TO MAKE A DUAL RACK MOUNT SET UP.

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, DUAL RACK/ ADAPTER	0102-00-1041	WVTK	0102-00-1041	1
NONE	JOINER, REAR PANEL	1400-01-5493	WVTK	1400-01-5493	1
NONE	SCREW, PAN, CAD I CROSS RECESS, 6-32 X 3/4	6-32 X 3/4 PAN	CMRCL	2800-38-6112	4
NONE	WASHER, SPLIT LOCK, #6	#6SRLW	CMRCL	2800-42-6000	4
NONE	EXTRUSION, TOP/ BOTTOM	MP-40951-0	BUKEY	3000-00-0099	2
NONE	HANDLE, DUAL RACK MOUNT	MP40110-2	BUKEY	3000-00-0100	2
NONE	EXTRUSION, FRONT SIDE	MP-40952-01	BUKEY	3000-00-0101	2

WAVETEK PARTS LIST	TITLE KIT, MODEL 270 DUAL RACK ADAPTER KIT	ASSEMBLY NO. 1101-00-1041 PAGE: 1	REV A

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 4/26/82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: DUAL RACK MOUNT 270 SERIES
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO 0102-00-1041 REV A
	SCALE NONE	CODE IDENT 23338	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3484

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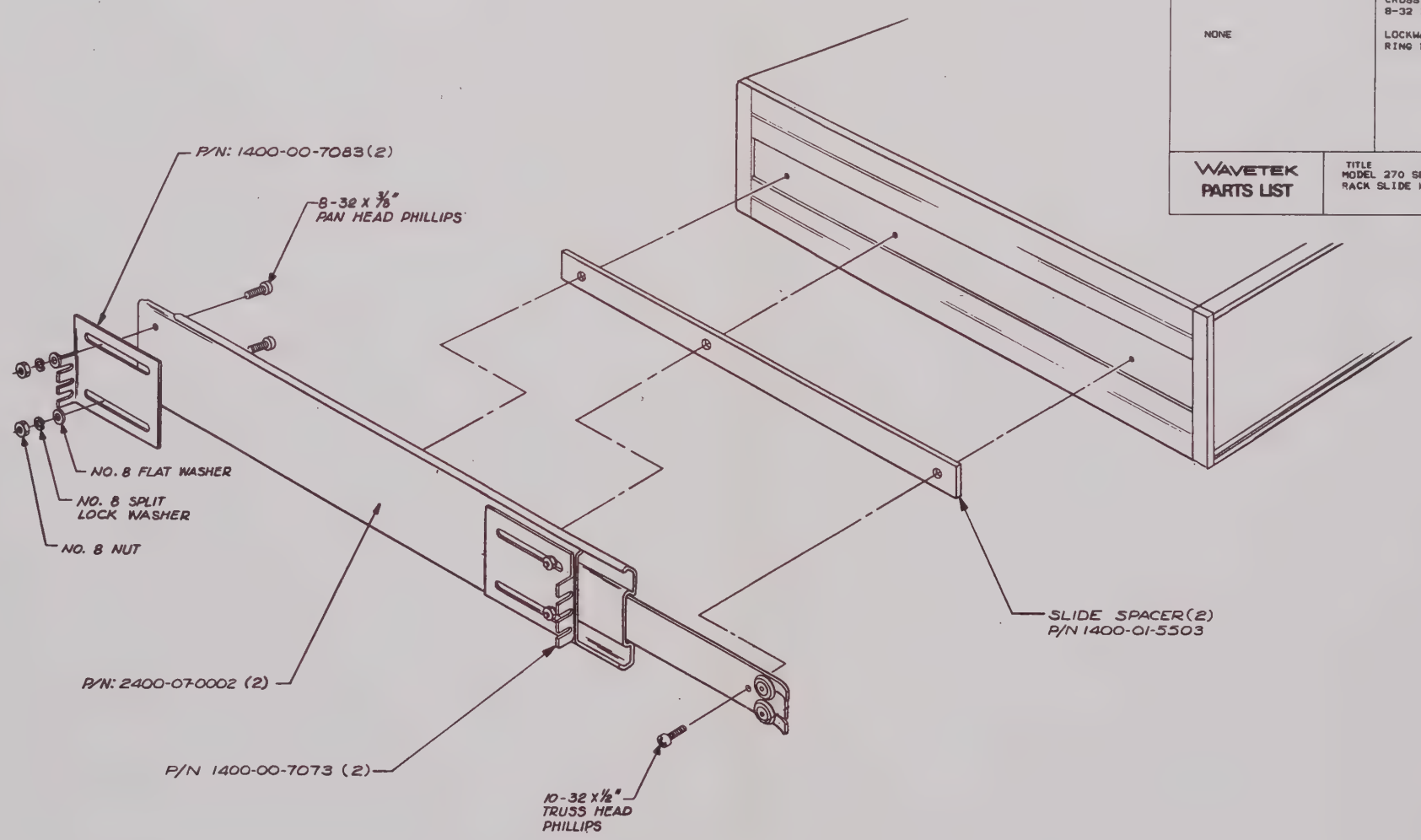
REFERENCE DESIGNATORS	PART DESCRIPTION	DRIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, RACK SLIDES	0102-00-1042	WVTK	0102-00-1042	1
NONE	EAR, RACK SLIDE	1400-00-7073	WVTK	1400-00-7073	2
NONE	EAR, RACK SLIDE	1400-00-7083	WVTK	1400-00-7083	2
NONE	SPACER, SLIDE	1400-01-5303	WVTK	1400-01-5303	2
NONE	SLIDES REF 2400-99-0002	1100D-20-1	NL	2400-07-0002	2
NONE	NUT, HEX, CAD I, 8-32	8-32 HEX NUT	CMRCL	2800-14-8100	8
NONE	SCREW, TRUSS HD, CROSS RECESS, 10-32X 3/8	10-32 X 3/8	CMRCL	2800-20-0106	4
NONE	WASHER, FLAT, #8	#8 FW	CMRCL	2800-26-8000	8
NONE	SCREW, PAN, CAD I, CROSS RECESS, 8-32 X 3/8	8-32 X 3/8 PAN	CMRCL	2800-38-8106	8
NONE	LOCKWASHER, #8 SPLIT RING BIN 540	#8SRLH	CMRCL	2800-42-8000	8

WAVETEK PARTS LIST	TITLE MODEL 270 SERIES RACK SLIDE KIT	ASSEMBLY NO. 1101-00-1042 PAGE: 1	REV A


P/N: 1400-00-7083(2)
8-32 X 3/8" PAN HEAD PHILLIPS
NO. 8 FLAT WASHER
NO. 8 SPLIT LOCK WASHER
NO. 8 NUT
P/N: 2400-07-0002 (2)
P/N 1400-00-7073 (2)
10-32 X 1/2" TRUSS HEAD PHILLIPS
SLIDE SPACER(2) P/N 1400-01-5303

TYP BOTH SIDES

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 9-30-87	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR KBI	7/15/87	TITLE ASSEMBLY, RACK SLIDE
FINISH WAVETEK PROCESS	RELEASE APPROV BH		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .03?		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO 0102-00-1042 REV
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

7-37

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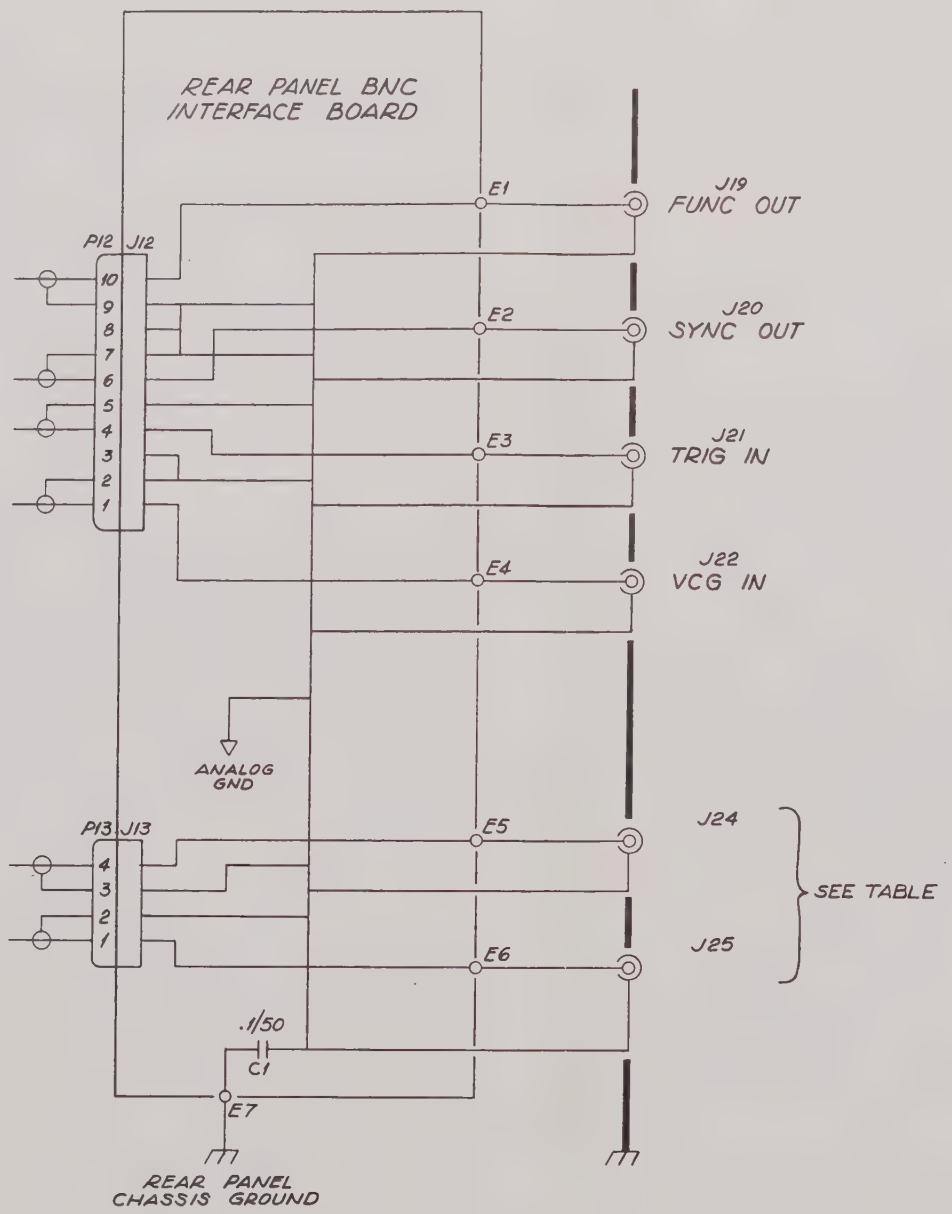
REV	ECN	BY	DATE	APP
A	# 3904	SC	8-8-83	



TABLE

MODEL	CONNECTOR	LABEL
270	J24	N/A
	J25	N/A
271	J24	N/A
	J25	N/A
273	J24	MARKER OUT
	J25	HORZ/GCV OUT
275	J24	ARB RTS/HOLD IN
	J25	ARB SYNC OUT
278	J24	REF IN
	J25	REF OUT

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, REAR PANEL BNC BOARD	0101-00-1010	WVTK	0101-00-1010	1
NONE	SCHEMATIC, REAR PANEL BNC BOARD	0103-00-1010	WVTK	0103-00-1010	1
C1	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1300-01-0405	1
10	REAR PANEL BNC BD	1700-00-1010	WVTK	1700-00-1010	1
6	CONNECTOR, HEADER (10 PIN)	102202-7	AMP	2100-02-0132	1
2	TERM, LOCK LUG	1414-8	SMITH	2100-04-0010	1

WAVETEK PARTS LIST	TITLE PCA, REAR PANEL BNC	ASSEMBLY NO. 1100-00-1010 PAGE: 1	REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN FN AQUINO 9/2/82	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	PROJ ENGR RBK 7/15/83	TITLE OPTION 002 REAR PANEL BNC'S	
FINISH WAVETEK PROCESS	RELEASE/APPROV	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030	
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO 0103-00-1010 REV A
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

B BHOP GRAPHICS ACCUPRESS REORDER NO. A 3894

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ANALOG INTERFACE

SAMPLE AND HOLD

DAC

-10.24V REF
R17 6.81K
-10.24V
TP1
+15V
R15 10K
R16 200
U16 CA082
-10.24 REF ADJ
C22 .1/50V +15V
ADRØ
U15 DAC 1006
C23 .1/50V
C24 .1/50V
-15V
CA082
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7

ANALOG DECODER

+5V
R14 2.2K SIP
ADR3
ADR4
ANALOG/
U14 1/2 LS139
ANAØ/
ANA1/
ANA2/
ANA3/

C21 .1/50V +5V
R14 2.2K SIP
ADRØ
ADR1
U14 1/2 LS139
ARØ/
AR1/
AR2/
AR3/

SAMPLE AND HOLD

1/4 DG211
U17
IN
U18 LS04
C25 .1/50V
C26 .1/50V
C27 22pF
C28 1mf POLYE
C29 910pF SM
C30 910pF SM
R18 301K
R19 301K
U19 CA082
C64 .1/50V
C65 .1/50V
C20 .1/50V
+5V +15V -15V

1/4 DG211
U17
U18 LS04
C31 22pF
C32 .1 POLYE
C33 910pF SM
C34 910pF SM
R20 301K
R21 301K
U19 CA082

1/4 DG211
U17
U18 LS04
C35 22pF
C36 .1 POLYE
C37 910pF SM
C38 910pF SM
R22 301K
R23 301K
U20 CA082
C66 .1/50V
C67 .1/50V

1/4 DG211
U17
U18 LS04
C39 22pF
C40 .1 POLYE
C41 910pF SM
C42 910pF SM
R24 301K
R25 301K
U20 CA082

BATTERY TEST

+15V
R26 12.4K
BATV
U27 CA082
R27 1M
R28 2.37K
-15V
R29 27.4K
CR6
PORT 15
R30 124K
PORT 14
R31 20K

ANALOG REGISTERS

ARØ/ U21 C374 ANLØ ANL1 ANL2 ANL3 ANL4 ANL5 ANL6 ANL7
AR1/ U22 C374 ANL8 ANL9 ANL10 ANL11 ANL12 ANL13 ANL14 ANL15
AR2/ U23 C374 ANL16 ANL17 ANL18 ANL19 ANL20 ANL21 ANL22 ANL23
AR3/ U24 C374 ANL24 ANL25 ANL26 ANL27
DATA Ø DATA 1 DATA 2 DATA 3 DATA 4 DATA 5 DATA 6 DATA 7
C43 C44 C45 C46 .1/50V +5V

AUX BUFFERS

U29 LS244
DATA Ø DATA 1 DATA 2 DATA 3 DATA 4 DATA 5 DATA 6 DATA 7
B DATA Ø B DATA 1 B DATA 2 B DATA 3 B DATA 4 B DATA 5 B DATA 6 B DATA 7

U28 LS244
PORT 12
ANA 2/
ANA 3/
N.C.
ADR Ø
ADR 1
ADR 2
N.C.
BANA 2/
BANA 3/
N.C.
B ADRØ
B ADR 1
B ADR 2
N.C.

DISPLAY

J7
+45V
+5V
KYBD/
PORT 21
PORT 16
DISP/
AD4 AD3 AD2 AD1 ADØ ADR3 ADR2 ADR1 ADRØ
DATA 7 DATA 6 DATA 5 DATA 4 DATA 3 DATA 2 DATA 1 DATA Ø
+15V

NOTE UNLESS OTHERWISE SPECIFIED

ANALOG

J6
SHO SH1 SH2 SH3
ANLO ANL1 ANL2 ANL3 ANL4 ANL5 ANL6 ANL7 ANL8 ANL9 ANL10 ANL11 ANL12 ANL13 ANL14 ANL15 ANL16 ANL17 ANL18 ANL19 ANL20 ANL21 ANL22 ANL23 ANL24 ANL25 ANL26 ANL27
PORT10
PORT 11

AUX

J4
BDATA0 BDATA1 BDATA2 BDATA3 BDATA4 BDATA5 BDATA6 BDATA7 BADR0 BADR1 BADR2 BANA2/ BANA3/
PORT13

REV	ECN	BY	DATE	APP

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN S.CHERMACK
DATE 8-2581
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC
MICRO-PROC/POWER SUPPLY
SERIAL NUMBERS BELOW 7230039

MODEL NO 271
DWG NO 0103-00-0919
REV
CAGE IDENT 23338
SHEET 2 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3884

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MICROPROCESSOR/MEMORY

GPIB INTERFACE

REV	ECN	BY	DATE	APP
	3374 (C.I.)			

MICROPROCESSOR

ADDRESS LATCH

GPIB ADDRESS

DATA LATCH

IEEE-488 INTERFACE

ALTERNATE BUS DRIVERS

IEE 488 BUS DRIVERS

ADDRESS DECODER

P/N 8600-00-0237

ROM

RAM

MASTER RESET

WRITE PULSE

TEST J8

1	E	18	AD7
2	ADR15	19	
3		20	AD6
4	ADR14	21	
5	AS	22	AD5
6	ADR13	23	TEST
7		24	AD4
8	ADR12	25	
9	NMI	26	AD3
10	ADR11	27	+5V
11		28	AD2
12	ADR10	29	N.C.
13		30	AD1
14	ADR9	31	N.C.
15		32	AD0
16	ADR8	33	
17		34	R/W

DS1 BEEPER QMB-06

U1 1/2 74LS00

U2 4040

Q1 2N3904

U3 6803

U4 74LS373

U5 74LS240

U6 68488

U7A 75160A

U7B 3447

U8A 75161A

U8B 3447

U9, U10 ROM

U11, U12 6116L RAM

U13

U25 74LS373

SW1

CR1 HP2811(2)

CR2 IN4148

CR4 MBR120

CR5 HP2811

BT1 STORED SETTING OPTION

Y1 4MHz

RESET

MR/

WRP/

KYBD/

DISP/

GPIB/

RAM2/

ROM1/

ROM2/

RAM1/

ANALOG/

BATV

PORT 10 PORT 11 PORT 12 PORT 13 PORT 14 PORT 15 PORT 16 PORT 17

PORT 21 PORT 22 PORT 20 N/C N/C

PORT EO

ADR0 ADR1 ADR2 ADR3 ADR4 ADR5 ADR6 ADR7

DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7

GA0 GA1 GA2 GA3 GA4 FPADEN

1 D101 2 D102 3 D103 4 D104 13 D105 14 D106 15 D107 16 D108

17 REN 9 IFC 8 DAC 7 RFD 6 DAV 5 EOI 11 ATN 10 SRQ

U6-28 U6-25 U6-16 U6-34 U6-32 U6-30 U6-17 U8A-18 U6-27 U6-23 U6-35 U6-33 U6-31 U6-29 U6-18 U6-26 U8A-19

18,19,20,21,22,23,24

IEEE-488 CONN J2

KEY

6	PROM'S PROGRAMMED PER MODEL, SEE PARTS LIST.
5.	LAST REFERENCE DESIGNATORS USED ARE: R54, C70, CR16, VR4, SW1, U29, Q1, BT1
4.	ALL CAPACITORS ARE SHOWN IN MICRO-FARADS.
3.	ALL RESISTORS ARE SHOWN IN OHMS.
2.	ALL DIODES ARE FD6666.
1.	REFERENCE DESIGNATORS SHOWN ARE PARTIAL, PREFIX WITH ASSEMBLY REF DES (A6).

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.CHERMACK	DATE 8/25/81	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE SCHEMATIC MICRO-PROC/POWER SUPPLY SERIAL NUMBERS BELOW 7230039
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 271	DWG NO 0103-00-0919 REV
	SCALE	CF 23338	SHEET 1 OF 3

7-39

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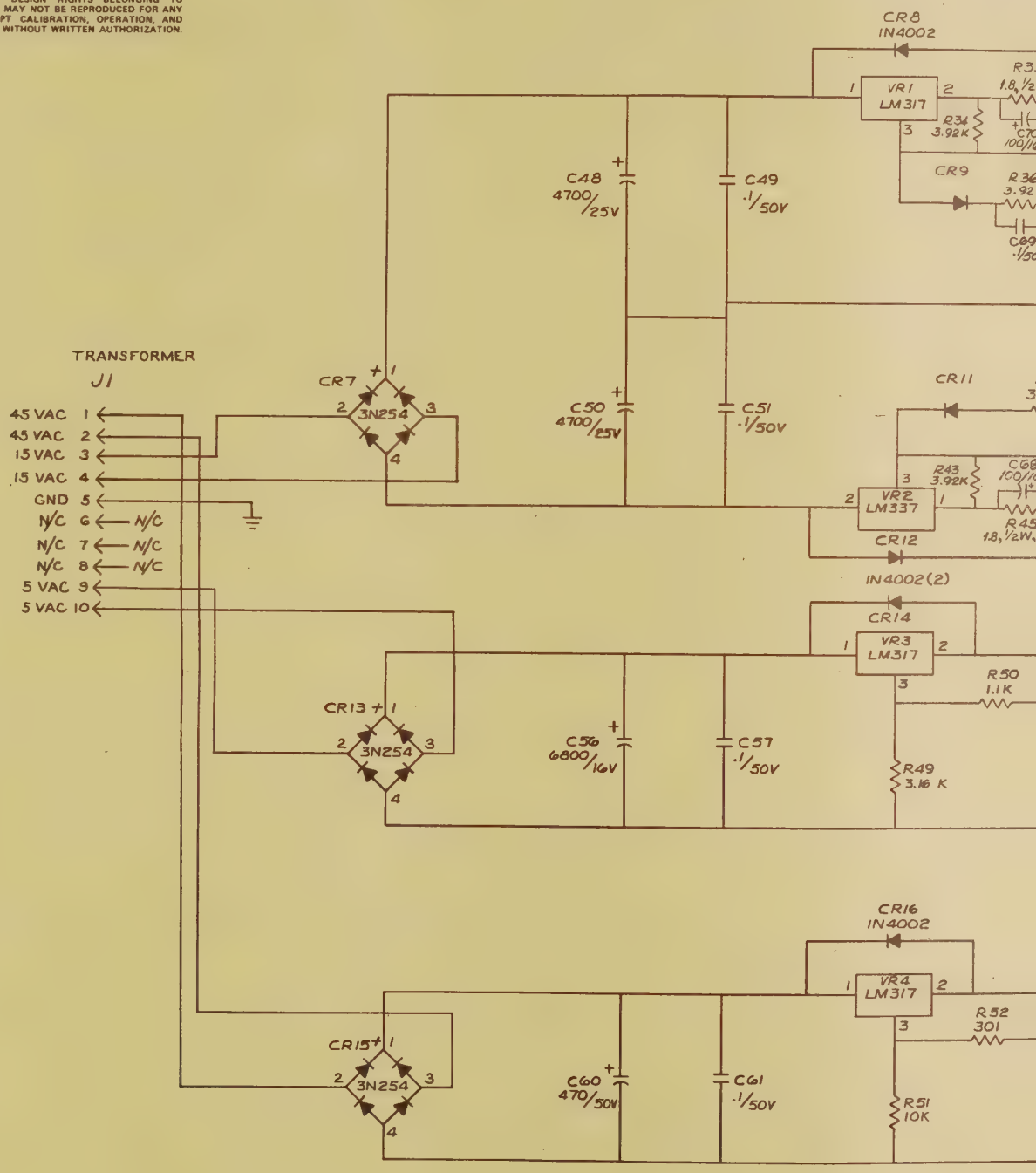
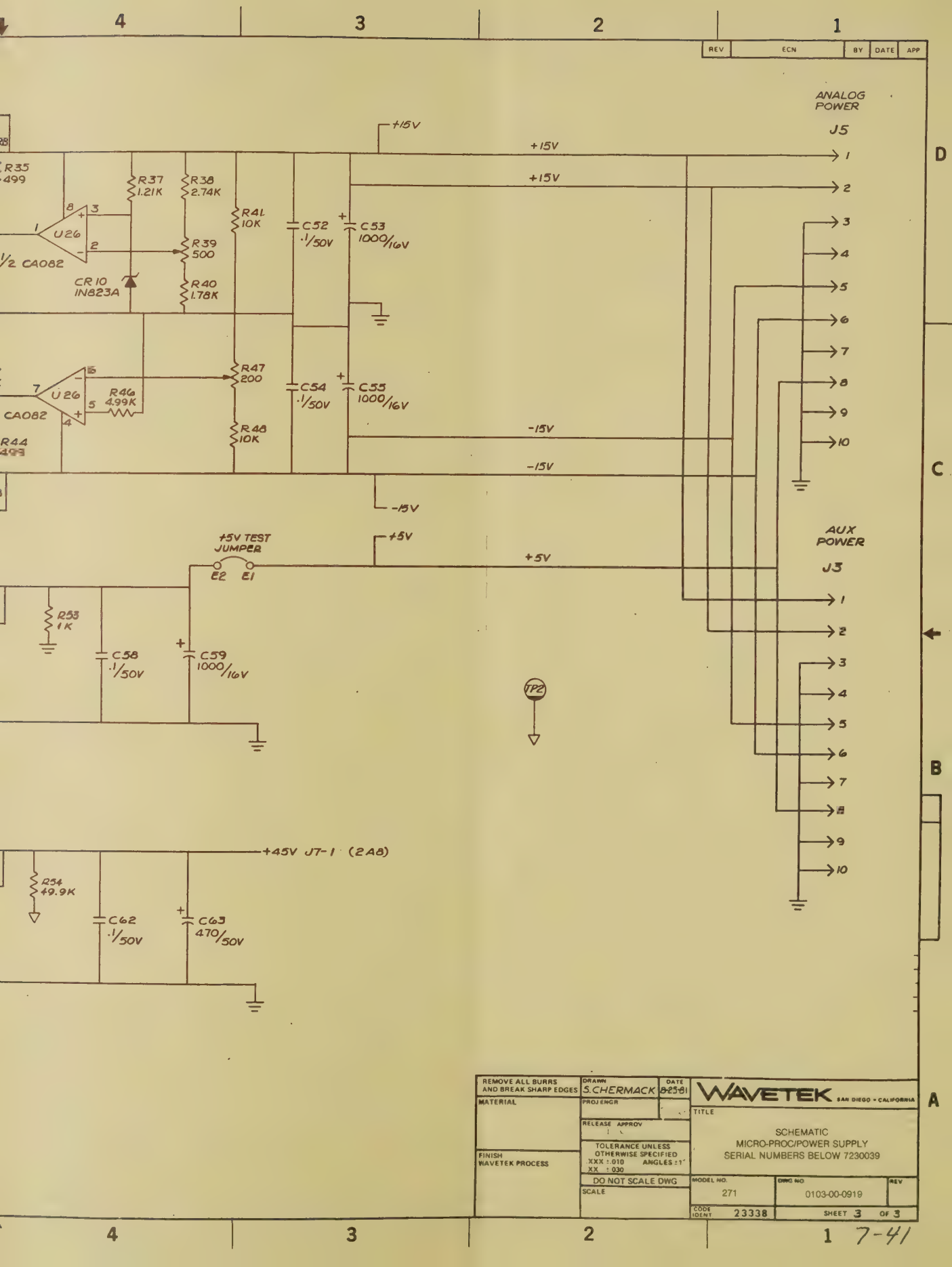
POWER SUPPLY



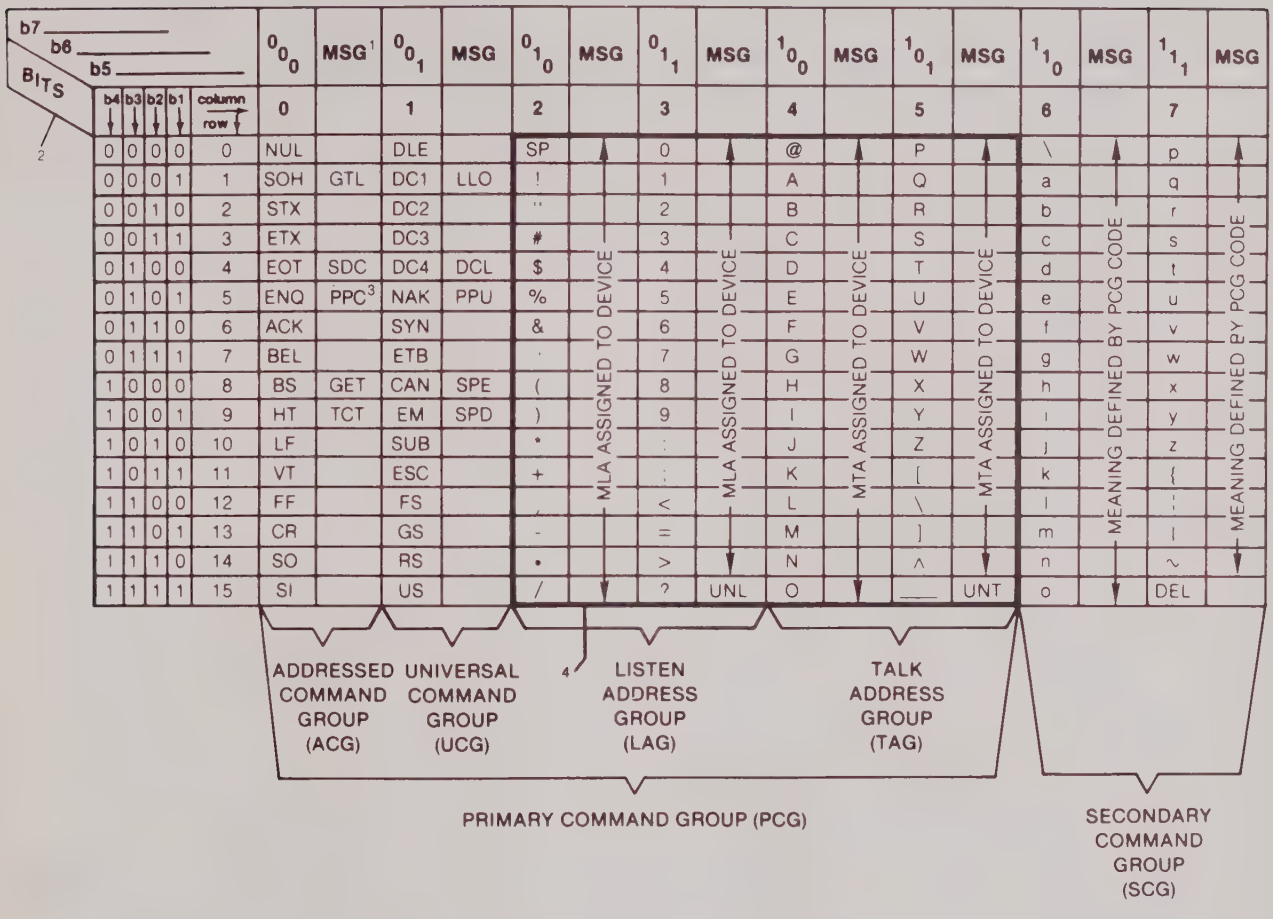
NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS
REORDER NO A-3004


4
3
2
1
REV
ECN
BY
DATE
APP
ANALOG POWER
J5
+15V
+15V
+15V
-15V
-15V
-15V
R35 499
R37 1.21K
R38 2.74K
R41 10K
C52 .1/50V
C53 1000/16V
U26
1/2 CA082
R39 500
CR10 IN823A
R40 1.78K
R47 200
C54 .1/50V
C55 1000/16V
U26
R46 4.99K
CA082
R48 10K
R44 499
+5V TEST JUMPER
E2
E1
+5V
+5V
AUX POWER
J3
R53 1K
C58 .1/50V
C59 1000/16V
TP2
+45V J7-1 (2A8)
R54 49.9K
C62 .1/50V
C63 470/50V
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN S.CHERMACK 8-25-81
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO - CALIFORNIA
TITLE
SCHEMATIC
MICRO-PROC/POWER SUPPLY
SERIAL NUMBERS BELOW 7230039
MODEL NO. 271
DWG NO 0103-00-0919
REV
CODE IDENT 23338
SHEET 3 OF 3
7-41

APPENDIX A

American Standard Code For Information Interchange (ASCII)



b4	b3	b2	b1	column / row	0	MSG[1]	1	MSG	2	MSG	3	MSG	4	MSG	5	MSG	6	MSG	7	MSG
0	0	0	0	0	NUL		DLE		SP		0		@		P		\		p	
0	0	0	1	1	SOH	GTL	DC1	LLO	!		1		A		Q		a		q	
0	0	1	0	2	STX		DC2		"		2		B		R		b		r	
0	0	1	1	3	ETX		DC3		#		3		C		S		c		s	
0	1	0	0	4	EOT	SDC	DC4	DCL	$		4		D		T		d		t	
0	1	0	1	5	ENQ	PPC[3]	NAK	PPU	%		5		E		U		e		u	
0	1	1	0	6	ACK		SYN		&		6		F		V		f		v	
0	1	1	1	7	BEL		ETB		'		7		G		W		g		w	
1	0	0	0	8	BS	GET	CAN	SPE	(		8		H		X		h		x	
1	0	0	1	9	HT	TCT	EM	SPD	)		9		I		Y		i		y	
1	0	1	0	10	LF		SUB		*		:		J		Z		j		z	
1	0	1	1	11	VT		ESC		+		;		K		[		k		{	
1	1	0	0	12	FF		FS		,		<		L		\		l		|	
1	1	0	1	13	CR		GS		-		=		M		]		m		}	
1	1	1	0	14	SO		RS		.		>		N		^		n		~	
1	1	1	1	15	SI		US		/		?	UNL	O		_	UNT	o		DEL	

[1]MSG = INTERFACE MESSAGE
[2]b1 = DIO1 . . . b7 = DIO7
[3]REQUIRES SECONDARY COMMAND
[4]DENSE SUBSET (COLUMN 2 THROUGH 5)

DC4	=	DCL	Device clear	Universal Command Group
DC1	=	LLO	Local lockout	
NAK	=	PPU	Parallel poll unconfigure	
EM	=	SPD	Serial poll disable	
CAN	=	SPE	Serial poll enable	
SOH	=	GTL	Go to local	Addressed Command Group
EOT	=	SDC	Selected device clear	
ENQ	=	PPC	Parallel poll configure	
BS	=	GET	Group execute trigger	
HT	=	TCT	Take control	

APPENDIX B

Programming Command Summary
(Excluding GPIB Command Groups Given in Appendix A)

Control and Data Names	Model 271 Key	ASCII Character (GPIB)
Change Sign	+/–	–
Decimal Point	•	•
0, 1, 2, . . . 9	0, 1, 2, . . . 9	0, 1, 2, . . . 9
Amplitude	AMPL	A
Mode	MODE	B
Function	FUNC	C
Offset	OFST	D
Exponent	EXP	E
Frequency	FREQ	F
Manual Trigger Released (Gate Off)	MAN (Released)	H
Execute	EXEC	I
Manual Trigger Pushed	MAN (Pressed)	J
Delay	DLY	L
Store Setting	STOR	M
Width	WID	N
Output Normal/Complement	COMP	O
Output On/Off	ON	P
Trigger Slope	SLP	Q
Burst	BRST	R
Period	PER	S
Upper Level	UPR	U
Lower Level	LWR	V
Recall Setting	RCL	Y
Reset	RST	Z
Percent Frequency	_____	XF
Get Mode	_____	XG
Trigger Level	LVL	XL
SRQ Mode	_____	XQ
Talk Mode	_____	XT
Recall Next Lesser Numbered Program	_____	XU
Terminator	_____	XV
Recall Next Greater Numbered Program	_____	XW
Cursor	↑, ↓, ←, →	_____
Clear Entry	CLR	_____
Beep On/Off	♪	_____
Display Test	DISP TEST	_____
Status Display	STAT	_____
Service Request	SRQ	_____
GPIB Address	ADRS	_____
Command Recall	CMD RCL	_____
Return to Local	LCL	_____

APPENDIX B (Continued)

Function (C) Code

0 Sine
1 Triangle
2 Square
3 Square Complement
4 DC
5 External Width
6 Single Pulse
7 Delay Pulse
8 Double Pulse

Main Generator Mode (B) Code

0 Continuous
1 Triggered
2 Gated
3 Burst

Normal/Complement (O) Code

0 Normal Pulse
1 Complement Pulse

Output On/Off (P) Code

0 Output Off, HI Z
1 Output On
2 Output Off, LO Z

Trigger Slope (Q) Code

0 Positive Edge
1 Negative Edge

GET Mode (XG) Codes

NOTE: This parameter selects which kind of action the 271 will take when it receives a GET command.

0 Execute and Trigger Upon Receipt of GET Command (No Error Checking).
1 Fetch Next Stored Setting, Execute and Trigger Upon Receipt of GET Command (No Error Checking).
−1 Fetch Previous Stored Setting, Execute and Trigger Upon Receipt of GET Command (No Error Checking).

SRQ (XQ) Code

NOTE: This parameter selects the conditions under which the SRQ line is asserted. Value can be 0 through 255. The equivalent binary value selects the response conditions as shown in table B-1 example.
Example: Binary 1 = Selected, Binary 0 = Not Selected.
XQ1 is the SRQ power-up mode. (The rsv bit is always asserted, selected or not.)

Talk Message (XT) Code

NOTE: This parameter selects the kind of message the 271 will send when it is addressed as a talker on the GPIB.

0 Programming Error list (only errors from GPIB input). 0 is the power-up talk mode. A typical error string is E 1F 2AD 3Y. Some error string characterics are:

a. All error strings begin with E.
b. Most recent error is at the end of string.
c. Errors are separated by blanks.
d. Class 1 Errors: A 1 followed by program ming character that caused the error.

Table B-1
Serial Poll Response Byte

Bit Weight	**128 (MSB)**	**64**	**32**	**16**	**8**	**4**	**2**	**1 (LSB)**
Bit Meaning	SRQ Key (Front Panel)	rsv	Undefined	Undefined	Low Battery	Fuse Blown	Output Protection	Program Error
Example*	1	0	0	0	0	0	0	1

Select Program Error and SRQ key (XQ129**)*

e. Class 2 Error: A 2 followed by the two conflicting program characters.

f. Class 3 Error: A 3 followed by M (Store) or Y (Recall).

g. Error strings can be up to 80 characters including E and blanks.

h. After transfer, the instrument clears the error string.

1. Poll Byte Response: The byte that would be sent if a serial poll was performed. The controller, upon reading this byte, clears the poll byte and resets the SRQ line if asserted.

2. The most recently selected parameter and its value. Example: FREQ 1E3. (The "most recently selected parameter" is the parameter at the end of the command string.) If no parameter is selected; e.g., power-on state or reset, or execute command then the instrument returns: NO PARAMETER SELECTED. Note that the NO PARAMETER SELECTED message will be returned if the last command in the string is an EXECUTE command (I).

3. The entire instrument setup after last execute. Example: F1E3A1D0C0P0Q0XL1.5.

4. The instrument setup when an execute is received; same format as XT3.

5. Instrument Identification: WAVETEK MODEL 271 V(X.Y). X.Y identifies the software version number.

6. The time since the instrument was powered on. Example Time: 1.3. Unit of measure is hours with 0.1 hour resolution (6 minutes).

7. The accumulated operating time. Example: TOTAL TIME: 306.2.

NOTE:

Toggling switch 7 (figure 2-2) clears the instrument-operating-time clock. With SW7 on, the clock runs during power on. With SW7 off, the clock clears to zero.

8. The number of stored settings installed, For the 271: STORED SETTINGS 150.

APPENDIX C
Displays

Key Pressed	Display - ACTUAL (Explanation)
ADRS	GPIB ADRS (Decimal address)
AMPL	AMPLITUDE (Value) (mV or V)
♪(beep)	(Audible beep)
BRST	BURST COUNT (Value)
CLR	(Clears any unexecuted numerical entry of the last parameter entered)
COMP	PULSE (NORMAL (0), COMP (1))
CMD RCL	(A string of letters and numbers up to 40 characters long displayed 20 characters at a time and shifted by the cursor ←, →)
CURSOR ←, →	(If a value is being displayed, the selected digit blinks. If there is no value being displayed, there is no effect. If it was a command recall, ← shifts the display four characters to the left. If it was a command recall, → shifts the display four characters to the right.
CURSOR ↑	(If the display is a value, code or storage location number, it increments.)
CURSOR ↓	(If the display is a value, code or a storage location number, it decrements.)
DLY	DELAY (value) (ns, μs or ms)
DISP TEST	(All display segments are lit.)
EXEC	EXECUTE (If no type 2 errors)
EXP	(If previous display was a value or a code, it is suffixed with an E.)
FREQ	FREQ (Value) (mHz, Hz, kHz or MHz)
FUNC	FUNC (Description) (Code)
LWR	LOWER LEVEL (Value) (mV or V)
MAN TRIG	(When pressed: No display if in continous mode, TRIGGER if in any triggered or burst mode, GATE if in gated mode.)

Under remote operation, certain characters may appear in the extreme right side of the display. Those characters are:

R — Remote
L — Addressed to Listen
T — Addressed to Talk
Q — Request for service because of selected SRQ code.

APPENDIX C (Continued)

Key Pressed	Display — ACTUAL (Explanation)
MODE	MODE (CONTINUOUS (0), TRIGGERED (1), GATE (2) or BURST (3))
PER	PERIOD (Value) (ns, μs, ms or s)
ON	OUTPUT (OFF (0); ON (1); or OFF, LO Z(2))
OFST	OFFSET (+ or −) (Value) (mV, V)
RCL	No. (Value) LAST RECALLED
RST	RESET or UNIT REMOTE (if in remote)
SLP	TRIG SLOPE (POS (0) or NEG (1))
STOR	No. (Value) LAST STORED
STAT	(Display changes automatically) FREQ (Value) (mHz, Hz, kHz or MHz) AMPLITUDE (Value) mV or V) OFFSET (Value) (mV or V) MODE (Mode) (Code) FUNC (Function) (Code) BURST COUNT (Value) PERIOD (Value) (ns, μs, or ms) DELAY (Value) (ns, μs or ms) WIDTH (Value) (ns, μs or ms) UPPER LEVEL (Value) (mV or V) LOWER LEVEL (Value) (mV or V) PULSE (Normal (0); or COMP (1)) OUTPUT (OFF (0); ON (1); or OFF, LO Z(2)) TRIG SLOPE (POS or NEG) (Code) TRIG LEVEL (+ or −) (Value) (mV or V)
UPR	UPPER LEVEL (Value) (mV or V)
(Number key)	(Number corresponding to the selected key.)
WID	WIDTH (Value) (ns, μs, or ms)

Functions

Code	Function (C)
0	Sine
1	Triangle
2	Square
3	Square Complement
4	DC
5	External Width
6	Single Pulse
7	Delayed Pulse
8	Double Pulse

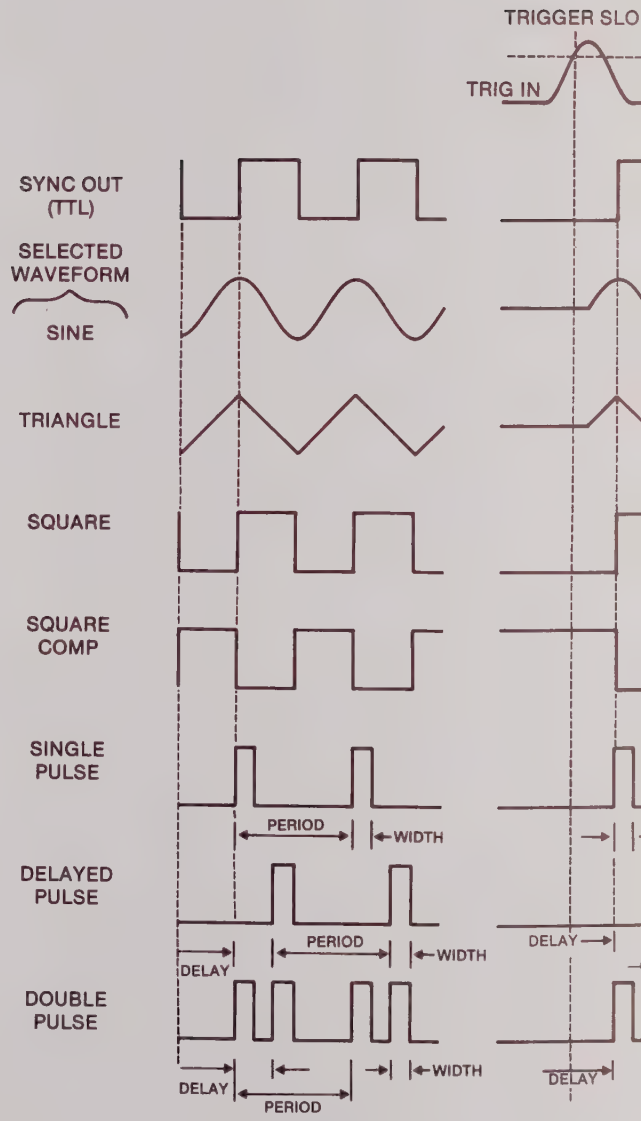
Recall Setting Menu

Recall (RCL)	Setting
RCL 0	RCL Last Power Off Condition
RCL 1-150	RCL User-Stored Settings
RCL 1000-1039	Internal Calibration Procedure
RCL 2000-2009	Internal QA Test/ Demonstration Procedure

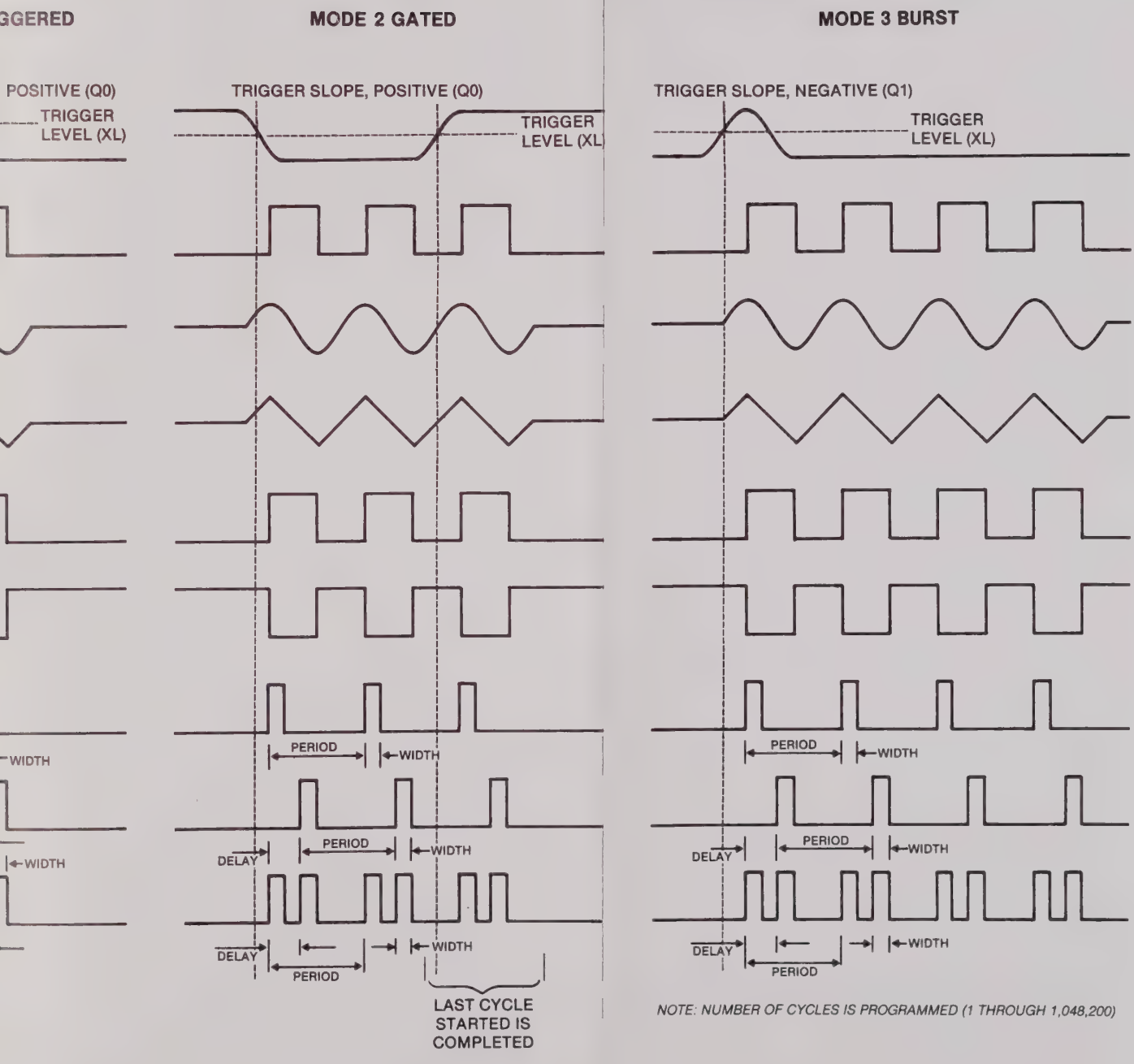
Operational Modes

Code	Mode (B)
0	Continuous
1	Triggered
2	Gated
3	Burst

MODE 0 CONTINUOUS **MODE 1 T**



ENDIX D
ming Reference Sheet



NOTE: NUMBER OF CYCLES IS PROGRAMMED (1 THROUGH 1,048,200)

APPENDIX E
Glossary of Mnemonics

Microprocessor/Power Supply Board

AD0 to AD7	Bidirectional, multiplex, 8 bit address/data bus from/to microprocessor
ADR0 to ADR15	16 bit address bus from microprocessor-lower 8 bits are latched from AD0 to AD7
$\overline{\text{ANA0}}$ to $\overline{\text{ANA3}}$	4 line address decoding for analog control lines to function generator and synthesizer board
$\overline{\text{ANALOG}}$	Decode line for analog section of memory
ANL0 to ANL27	28 analog logic signals to function generator board
$\overline{\text{AR0}}$ to $\overline{\text{AR3}}$	4 line address decoding to analog registers for function generator board control lines
AS	Address strobe from microprocessor
ATN	IEEE-488 "attention"
BADR0 to BADR2	3 buffered address lines to synthesizer board
BATV	Battery voltage
BDATA0 to BDATA7	8 bit, buffered, latched data bus to synthesizer board
DI01 to DI08	8 bit, IEEE-488 data bus
DAC	IEEE-488 "data accepted"
DATA0 to DATA7	8 bit, latched data bus for control lines to the display, sample and hold, and analog interface
DAV	IEEE-488 "data valid"
$\overline{\text{DISP}}$	Decode line for display section of memory
E	Enable line from microprocessor
EOI	IEEE-488 "end or identify"
FPADEN	Front panel GPIB address entry switch
GA0 to GA4	GPIB address switches corresponding to 2^0 through 2^4 respectively. (1 through 16) adding to 31 maximum
$\overline{\text{GPIB}}$	Decode line to select the IEEE-488 interface (general purpose interface bus)
IFC	IEEE-488 "interface clear"
$\overline{\text{KYBD}}$	Decode line to select keyboard
$\overline{\text{MR}}$	Master reset to initialize microprocessor
$\overline{\text{NMI}}$	Non-maskable interrupt line to microprocessor
PORT 10 to PORT 17	8 line I/O port 1 to/from microprocessor
PORT 20 to PORT 24	5 line I/O port 2 to/from microprocessor
$\overline{\text{RAM1}}$ to $\overline{\text{RAM2}}$	Address decode lines for random access memory ICs 1 and 2
REN	IEEE-488 "remote enable"
RFD	IEEE-488 "ready for data"
$\overline{\text{ROM1}}$ to $\overline{\text{ROM2}}$	Address decode lines for read-only memory ICs 1 and 2
R/$\overline{\text{W}}$	Read/write line from microprocessor
SH0 to SH3	4 sample-and-hold analog signals to function generator board

APPENDIX E (Continued)

SRQ	IEEE-488 "service request"
TEST	Control line to allow operation with external test program—not normally used
$\overline{WRP}$	Write pulse to RAM

Display Board (Excluding Mnemonics Common to Microprocessor/Power Supply Board)

ANOA to ANOO & ANODP	Vacuum fluorescent display anodes corresponding to 14 segments, comma, and decimal point, respectively
$\overline{BLANK}$	Blanking control for display and scan clock
DSP	Display synchronizing pulse for shift register scan
GRID 1 to GRID 20	Display grids controlling each digit

Function Generator Board

AMP	Analog control voltage for amplitude (SH1)
AMPLDC	XY multiplier feedback of amplitude control dc test line
$\overline{CPM}$	Capacitance multiplier select line (ANL15)
$\overline{DCA}$	DC amplifier select line (ANL13)
DCCOMP	DC compensation and low frequency linearity correction for triangle buffer test line
EXW	External width select line (ANL18)
$\overline{FR0}$ to $\overline{FR7}$	Frequency range select lines to range capacitors, capacitance multiplier, and frequency compensation (ANL0 to ANL7)
FRQ	Analog control voltage for frequency (SH0)
FUB	Signal to microprocessor that output fuse is blown (PORT11)
MC0 and MC1	2 mode control lines (ANL11 and ANL12)
OA0 and OA2	2 output attenuator control lines (ANL8 and ANL10)
OAP	Signal to microprocessor that the output amplifier protection circuit is operating (PORT10)
OST	Analog control voltage for offset (SH2)
$\overline{OVR}$	Frequency overrange select line (ANL14)
PATEST	Preamplifier output test line
PLS	Pulse input select line (ANL25)
$\overline{PLS}$	Pulse complement select line (ANL24)
PLSI	Pulse input from pulse board
$\overline{RCT}$	Rectangular waveform select line—square or pulse (ANL23)
$\overline{SIN}$	Sine wave select line (ANL21)
SQB	Output from square buffer
SQR	Square wave select line (ANL20)
$\overline{SQR}$	Square complement select line (ANL19)
SQS	Square buffer to square logic signal
THC	Trigger holding current
TRB	Triangle buffer output
TRGI	Trigger input from pulse board
TRGO	Trigger output from pulse board
$\overline{TRI}$	Triangle wave select line (ANL22)
TRITST	Triangle buffer output test line

APPENDIX E (Continued)

TRL	Analog control voltage for trigger level (SH3)
TRN	Triangle generation current node
VCGI	Not used in Wavetek 271
VCGO	Not used in Wavetek 271
VCGTST	Voltage control generation circuit test line
VCV	Voltage control generation circuit voltage output
XYI	X-Y multiplier input
+I	Tracking current (I) source from VCG
−I	Tracking current (I) sink to VCG
+TR	Rising edge trigger select line (ANL17)
−TR	Falling edge trigger select line (ANL16)

Pulse Board

$\overline{\text{ANA2}}$	Control line from microprocessor. Logic low enables address decoder U1.
$\overline{\text{ANA3}}$	Control line from microprocessor. Logic low writes data from data bus into DAC U16 or U25 when the DAC is enabled by the appropriate address line.
BADR0-BADR2	Buffered address lines from microprocessor to address decoders U1 and DACs U16 and U25.
BDATA0-BDATA7	Buffered data bus from microprocessor board via J16 digital interface connector.
B0-B19	Preset data lines for burst counter.
BURST	Burst counter control line; logic high enables burst counter.
$\overline{\text{BURST}}$	Logic complement of BURST line; is at logic low in burst mode.
DELON	Control line from data latches to delay one-shot circuit. Logic high enables delay circuit; line is high for delayed pulse and double pulse, low for undelayed pulse.
$\overline{\text{DELPLS}}$	Control line from data latches to double pulse logic. Logic low on this line inhibits SQS square wave from triggering width one-shot circuit. (Width one-shot can be triggered only by delay one-shot circuit.) Line is at logic high for undelayed pulse and double pulse; at logic low for delayed pulse.
DEL-TOWID	Line from delay one-shot circuit to width one-shot circuit. Line is pulsed high by double pulse logic to trigger width circuit.
$\overline{\text{DR0}}$-$\overline{\text{DR7}}$	Control lines from data latches to select delay ranges in delay one-shot circuit.
PLSI	Pulse output from pulse board to function generator board.
SQS	Logic level square wave output of function generator board; used as input to burst counter and delay one-shot circuit.
TRGI	Output from burst counter circuit to trigger logic on function generator board.
TRGO	Trigger output from function generator board to burst counter circuit.
+VR10V	Regulated +10V from ±10 volt reference circuit; used as reference voltage to Digital-to-Analog Converters U16 and U25.
−VR10V	Regulated −10V from ±10 volt reference circuit; not used.
$\overline{\text{WR0}}$-$\overline{\text{WR7}}$	Control lines from data latches to select width ranges in width one-shot circuit.

APPENDIX F
Waveform Measurements

Frequency Jitter Measurement

Frequency jitter is defined as the cycle to cycle variation in period. Using a scope (with time base multiplier) display a square wave such that one cycle covers more than half the display (see figure F-1). Trigger the scope internally on the leading edge of signal. Using the time base multiplier expand the leading edge of the cycle after trigger by a factor of 100. Jitter is the peak to peak horizontal excursion of the displayed edge (see figure F-2). % jitter is given by:

$$\% \text{ Jitter} = (\text{Jitter/Period}) \times 100$$

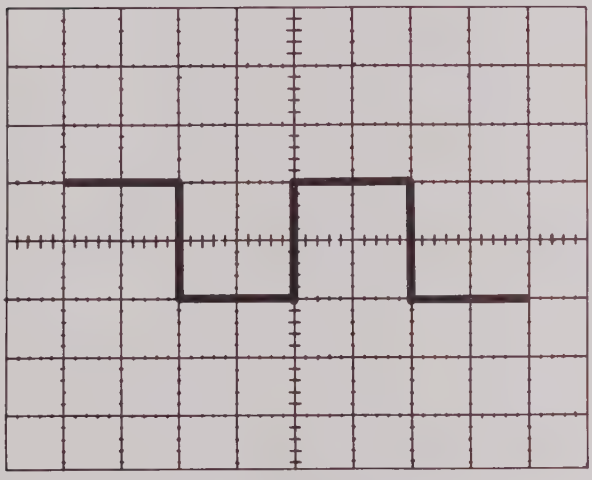


Figure F-1.

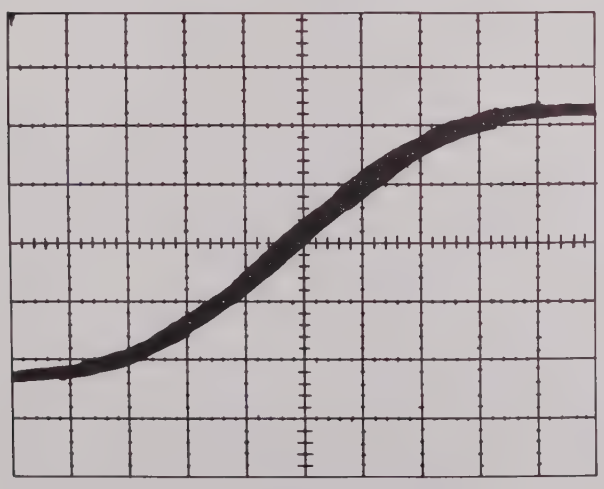


Figure F-2.

This test method is accurate for jitter caused by random or non-coherent noise sources. Coherent (harmonically related) cycle-to-cycle jitter requires unique verification.

Amplitude Measurements

There are several factors to be considered when making amplitude measurements. The type of DVM, the frequency range over which the meter is accurate, and the accuracy of the 50Ω load used for termination are the most important.

1. There are three basic types of DVM's: Averaging, true rms, and averaging scaled. The readings obtained can vary by more than 10% depending on DVM type and the waveform. The correct readings (related to volts peak to peak) are given below for each type of meter and each waveform.

   Average Reading:

Function	Reading
Sine	Vp-p/π
Triangle	Vp-p/4
Square	Vp-p/2

   True RMS:

Function	Reading
Sine	Vp-p/2$\sqrt{2}$
Triangle	Vp-p/2$\sqrt{3}$
Square	Vp-p/2

   Averaging Scaled: This type of meter measures internally like an average reading meter, but the displayed reading is scaled (multiplied by a constant) to read like a true rms meter. This scaling technique only works on sine waveforms; however, it gives less obvious results for other waveforms. The correct readings are given below:

Function	Reading
Sine	Vp-p/2$\sqrt{2}$
Triangle	(Vp-p × 1.1107)/4
Square	(Vp-p × 1.1107)/2
	or
Triangle	(Vp-p/4) × 1.1107
Square	(Vp-p/2) × 1.1107

2. Most ac volt meters have a relatively limited range of frequencies over which the meter is most accurate. For most meters this range is

about 500 Hz-5 kHz. In order to make accurate measurements the basic accuracy of the meter in its specified frequency operating range should be less than 0.2%.

3. The 50Ω load used to terminate the signal being measured can also introduce significant errors into the amplitude accuracy measurement. In general the measurement will be in error by 1/2% for every 1% error in the load. Standard loads available from Tektronix are ±2% accuracy. Therefore up to 1% error in amplitude measurement can result when using these loads. It is recommended to use a 0.1% accurate termination or to compensate the readings obtained based on the actual load value. The method for doing this is given below.
   a. Let R be the value of the termination.
   b. Let K be the correction factor applied to the DVM reading:

      Then: (correct reading) = (DVM reading) × K

      where $K = \frac{R+50}{2R}$

   Using this method the load tolerance can be ±5%.

Symmetry Measurements

1. Symmetry defined as a percentage is the ratio of positive half cycle time to the period (see figure F-3):

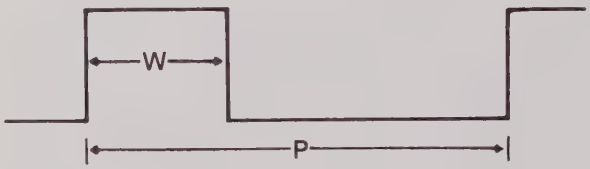


Figure F-3.

Where: % symmetry = (W/P) × 100

2. Symmetry error is, therefore, the difference from 50% symmetry:

   % Symmetry Error = [(½P—W)/P] × 100

3. When using a scope and alternately triggering on + and − slope of signal the symmetry error measured is twice the actual error. Therefore, when using this method the measured error must be divided by 2. Also, this method is only accurate at frequencies where the rise and fall time is not a significant part of the period. The period should be about 1000 times greater than the rise/fall time. This is about 10 μs or 100 kHz.
4. To measure symmetry at 12 MHz a different technique must be used. Connect signal (terminated into 50Ω) to a sampler set at 10 ns/div. Upper and lower levels should be exactly centered about horizontal centerline on scope display (see figure F-4). Rising edges of first and second cycle should be exactly equidistant from vertical center line. The distance of the falling edge from the vertical center line at the point falling edge crosses horizontal center line is the symmetry error.

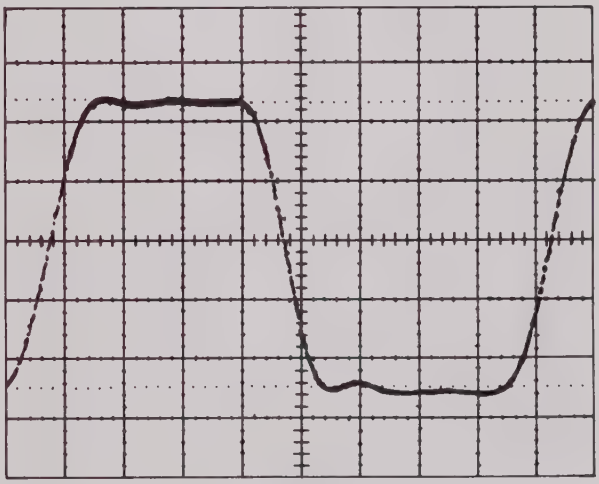


Figure F-4.

Waveform Quality Measurement

Waveform quality measurements should always be made using a sampling oscilloscope with precision 50Ω termination and cabling. Standard RG58 coax cable is not good enough for waveform quality measurements. Percent aberration is the ratio of absolute peak-to-peak variation from the 0% (negative level) or 100% (positive level) point on the square waveform to the absolute peak-to-peak amplitude of the square wave. See figures F-5, F-6 and formula shown below. In order to get an accurate display the top (or bottom) of the waveform should be expanded both vertically and horizontally to fill the scope display. The pictures below were made on a 5 Vp-p square waveform at 3 MHz and the scope horizontal and vertical were set to 20 ns/div and 100 mV/div respectively. Also, best

results are obtained when using the low noise (averaging) setting on the sampling scope.

$$\% \text{ ABERRATION} = \frac{|PK - PK\ VAR|}{|PK - PK\ SQWA|} \times 100$$

SQWA = SQUARE WAVE AMPLITUDE

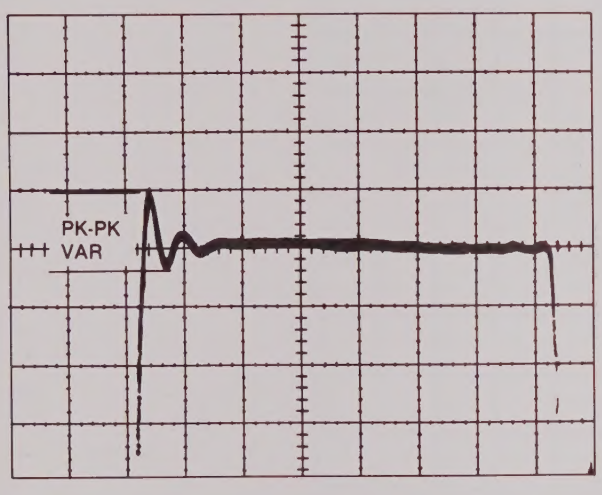


Figure F-5.

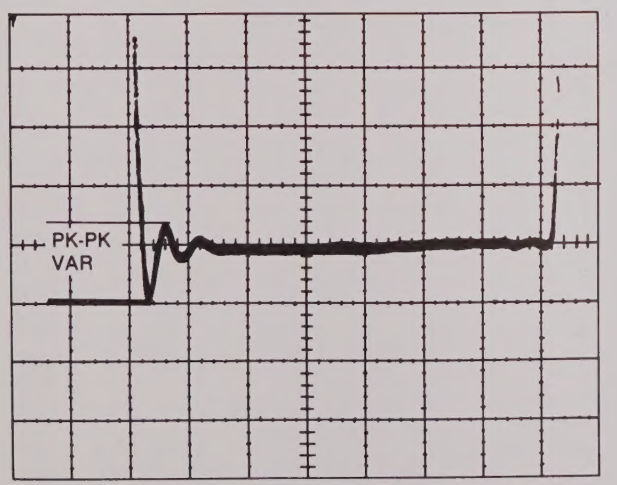


Figure F-6.

Width Measurement

Width is measured from the 50% point of the leading edge of the pulse to the 50% point of the trailing edge (see figure F-7). The pulse at the function out must be loaded into 50Ω. The upper and lower levels of the pulse must be set to +1V and −1V respectively. This makes the 50% points 0.0V on both leading and trailing edges of the pulse. The width duty cycle must be less than 33%.

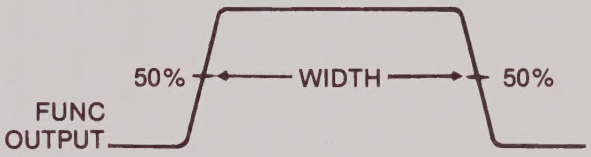


Figure F-7.

NOTE

The above definition applies to width settings less than 10μs. For width settings above 10μs the trigger points, upper level, lower level, and loading are unimportant, but the duty cycle criteria must still be followed.

Width Duty Cycle Definition

Defined as a percentage, width duty cycle is the ratio of width to the minimum period that does not cause pulse dropout:

$$\% \text{ DUTY CYCLE} = (\text{WIDTH/MIN PERIOD}) \times 100$$

For example, if width were set to 100 ns and the minimum period that could be programmed before pulse dropout occurred was 163 ns then the duty cycle would be:

$$\% \text{ DUTY CYCLE} = (100E\text{-}9/163E\text{-}9) \times 100$$
$$\% \text{ DUTY CYCLE} = 61.3\%$$

Width Jitter Measurement

Width jitter is defined as the pulse to pulse variation in pulse width. Using a scope (with time base multiplier) display one pulse on scope display so the pulse covers at least half of display (see figure F-8). Scope must be triggered internally on leading edge of pulse (not sync out). Using the time base multiplier expand the trailing edge of pulse by a factor of 100. Jitter is measured as the peak to peak horizontal excursion of the trailing edge (see figure F-9). % Jitter is:

$$\% \text{ Jitter} = (\text{Jitter/Width}) \times 100$$

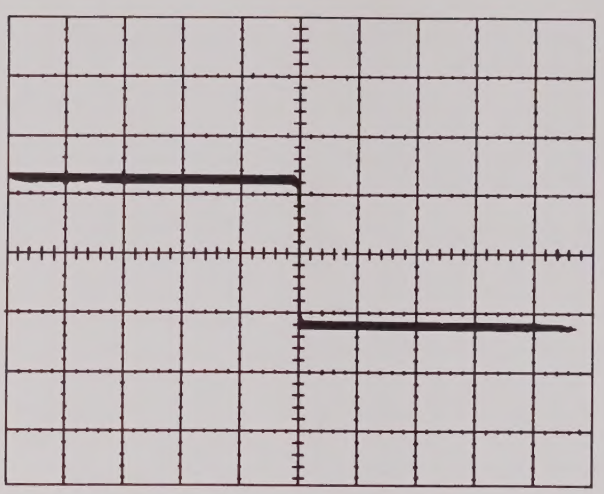


Figure F-8.

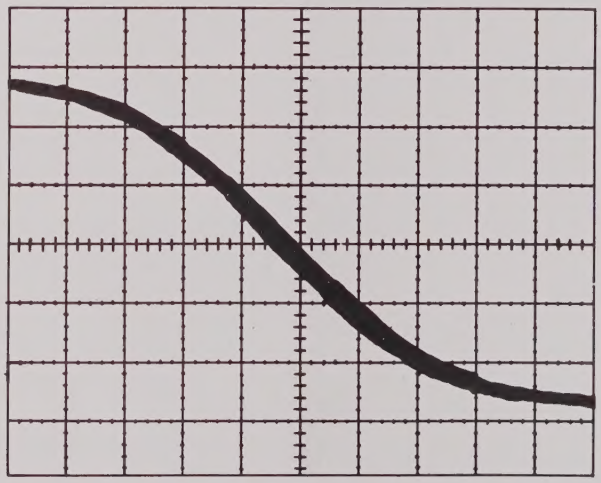


Figure F-9.

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